FIG. 1

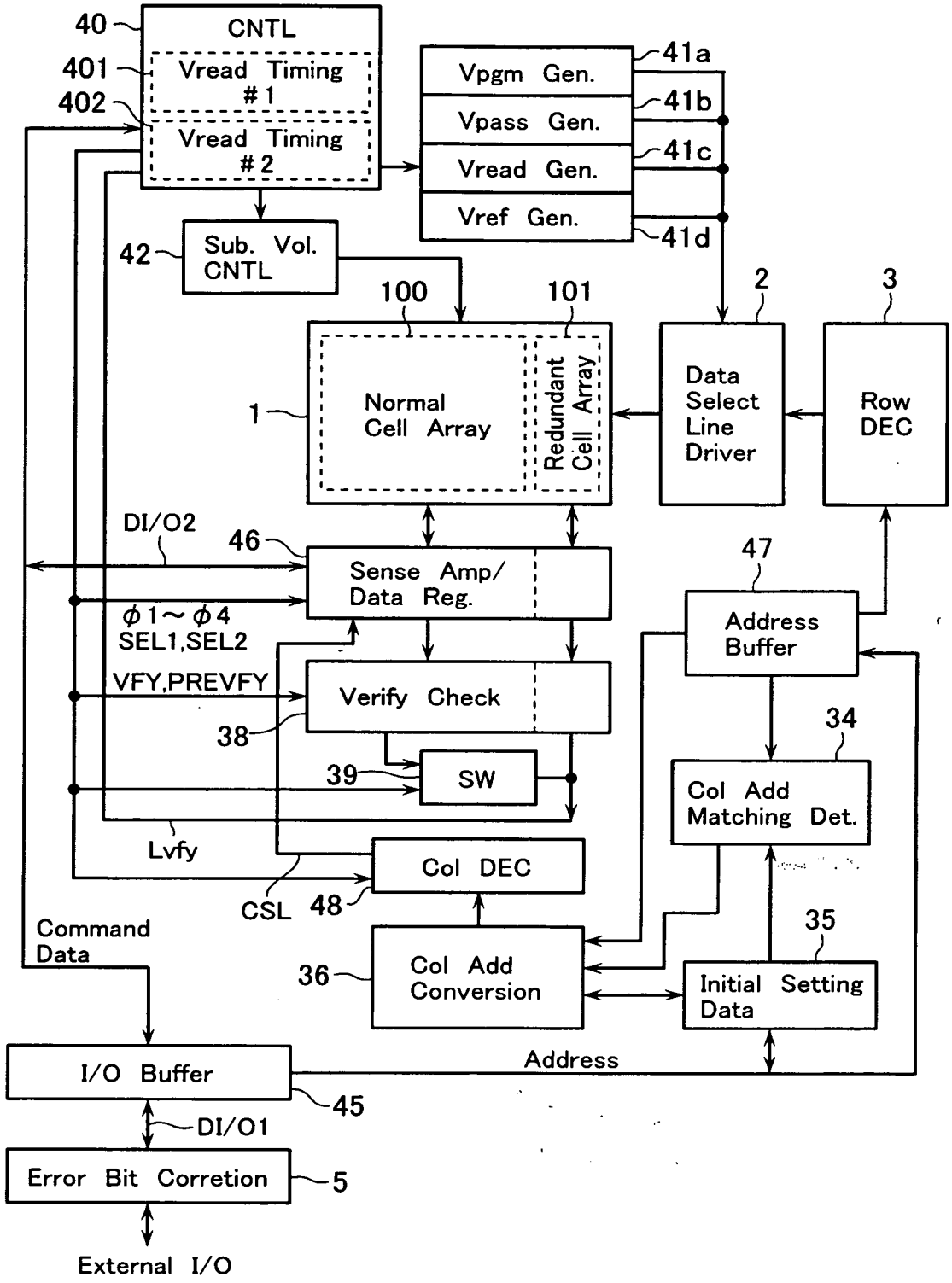

40
CNTL
401
Vread Timing #1
402
Vread Timing #2
Vpgm Gen.
Vpass Gen.
Vread Gen.
Vref Gen.
41a
41b
41c
41d
42
Sub. Vol. CNTL
100
101
2
3
1
Normal Cell Array
Redundant Cell Array
Data Select Line Driver
Row DEC
DI/O2
46
Sense Amp/ Data Reg.
47
Address Buffer
φ1～φ4
SEL1,SEL2
VFY,PREVFY
Verify Check
38
34
39
SW
Col Add Matching Det.
Lvfy
Col DEC
CSL
48
Command Data
35
36
Col Add Conversion
Initial Setting Data
I/O Buffer
Address
45
DI/O1
Error Bit Corretion
5
External I/O

FIG. 2A

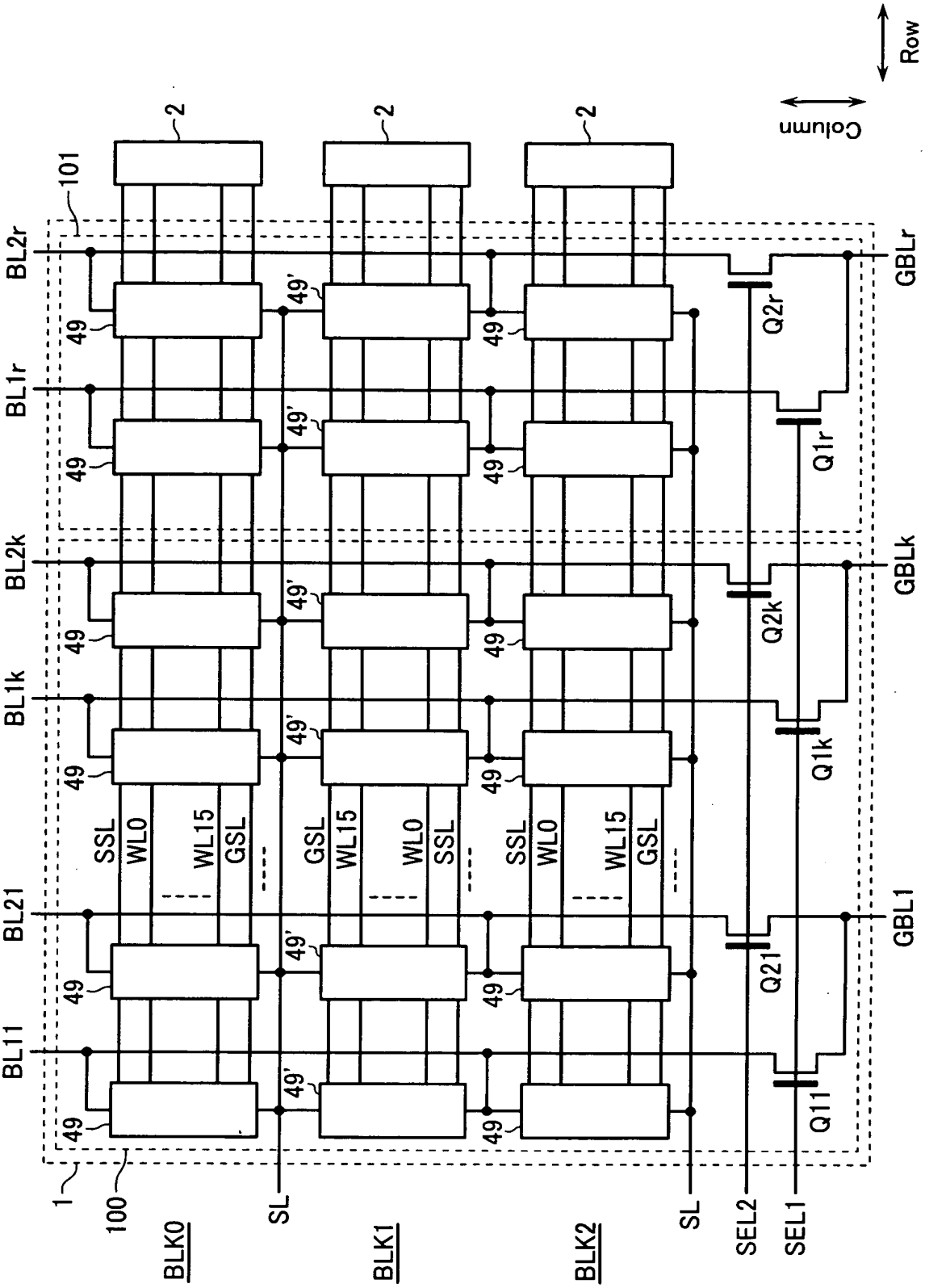
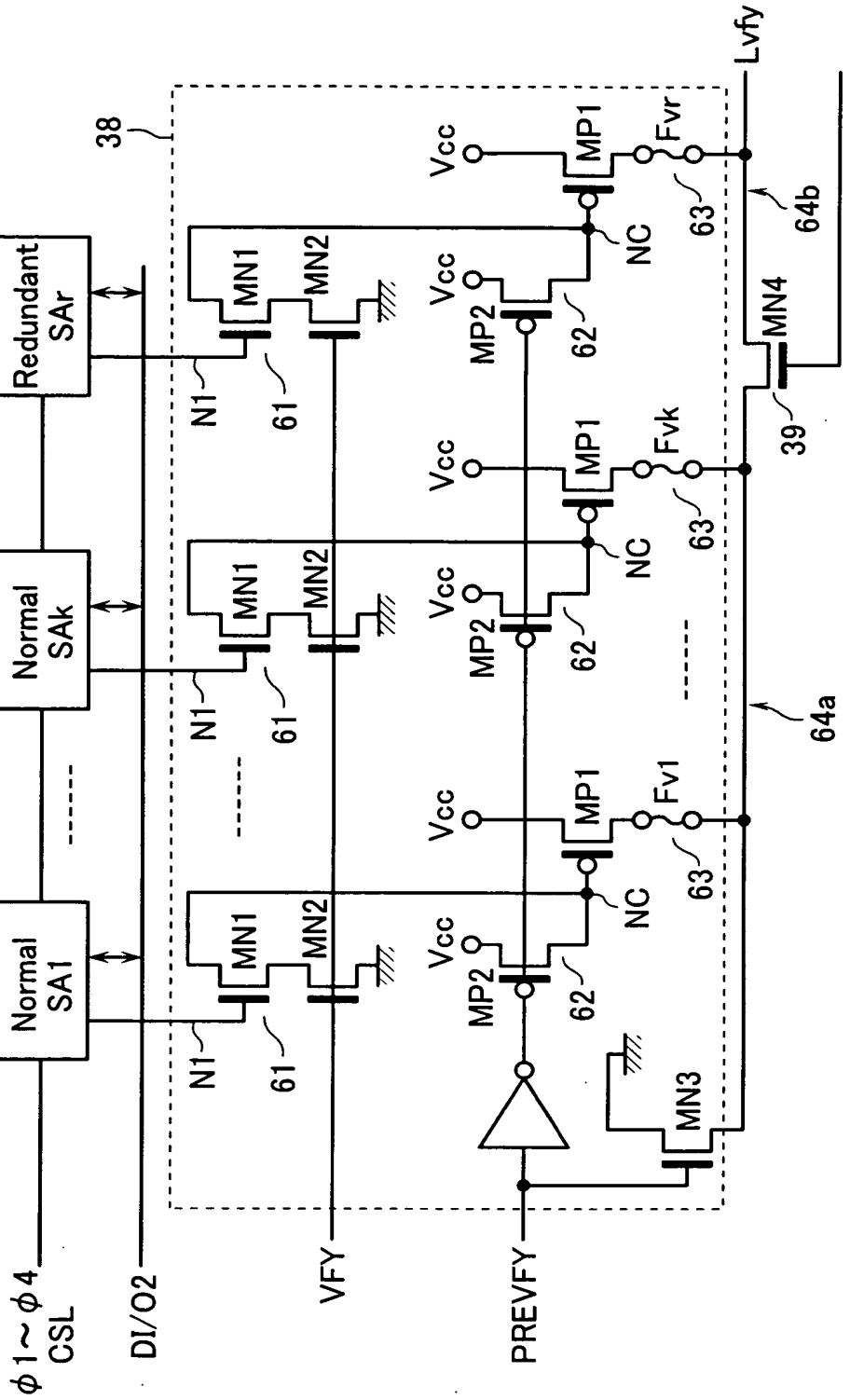

Row
Column
2
101
BL2r
BL1r
BL2k
BL1k
BL21
BL11
GBLr
GBLk
GBL1
Q2r
Q1r
Q2k
Q1k
Q21
Q11
49
49'
SSL
WL0
WL15
GSL
1
100
SL
BLK0
BLK1
BLK2
SEL2
SEL1

FIG. 2B


38
GBLr
GBLk
GBL1
46
Redundant SAr
Normal SAk
Normal SA1
N1
61
MN1
MN2
Vcc
MP2
MP1
62
NC
63
Fvr
Fvk
Fv1
Lvfy
64b
64a
MN4
39
MN3
φ1~φ4
CSL
DI/O2
VFY
PREVFY

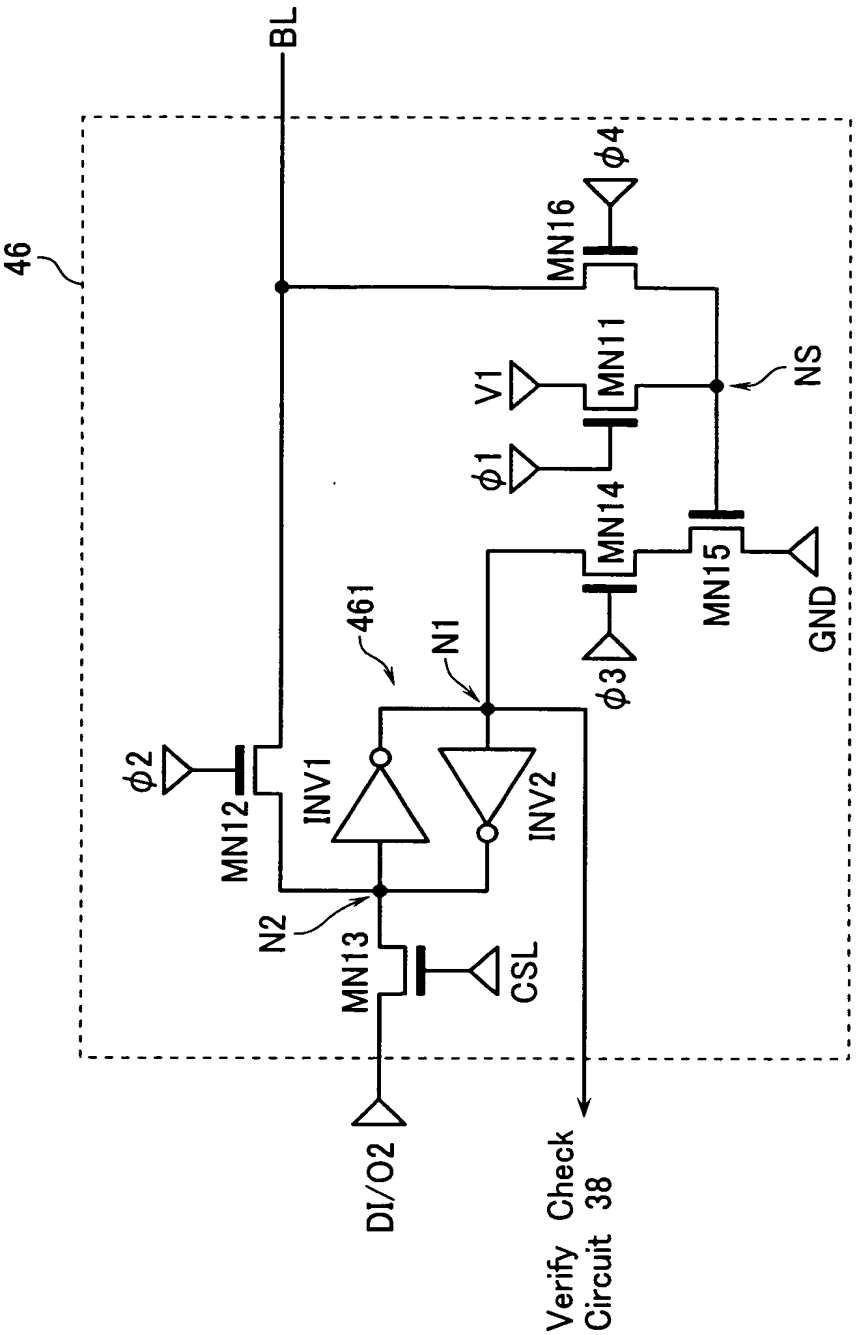

BL
46
MN16
φ4
V1
MN11
NS
φ1
MN14
MN15
GND
φ3
461
N1
φ2
MN12
INV1
INV2
N2
MN13
CSL
DI/O2
Verify Check
Circuit 38

FIG. 3

FIG. 4

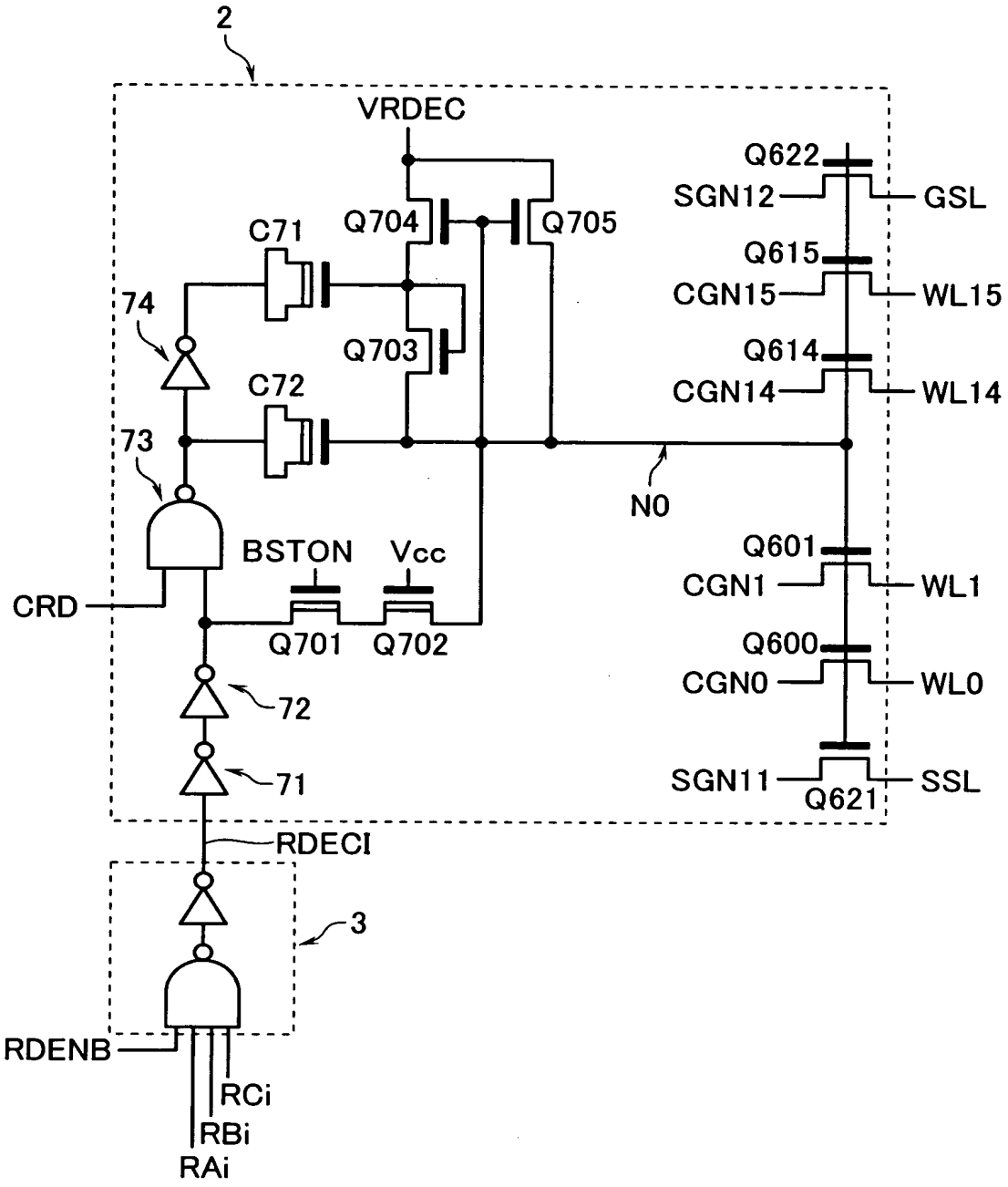

2
VRDEC
Q622
SGN12
GSL
Q615
CGN15
WL15
Q614
CGN14
WL14
Q601
CGN1
WL1
Q600
CGN0
WL0
SGN11
Q621
SSL
C71
Q704
Q705
74
Q703
C72
73
N0
BSTON
Vcc
CRD
Q701
Q702
72
71
RDECI
3
RDENB
RCi
RBi
RAi

FIG. 5

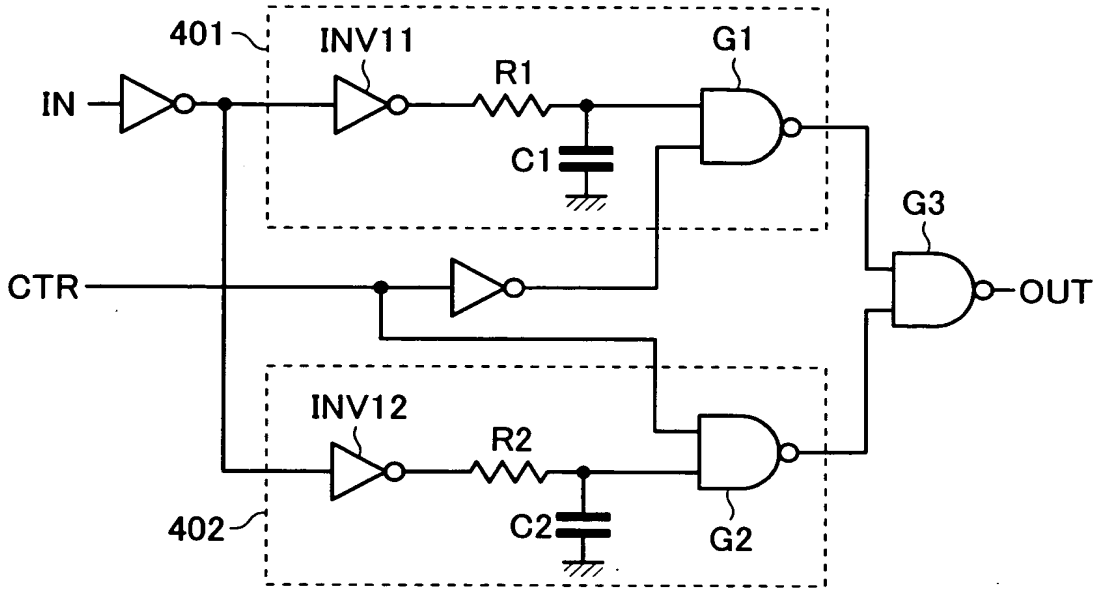

401
INV11
R1
G1
IN
C1
G3
CTR
OUT
INV12
R2
402
C2
G2

FIG. 6

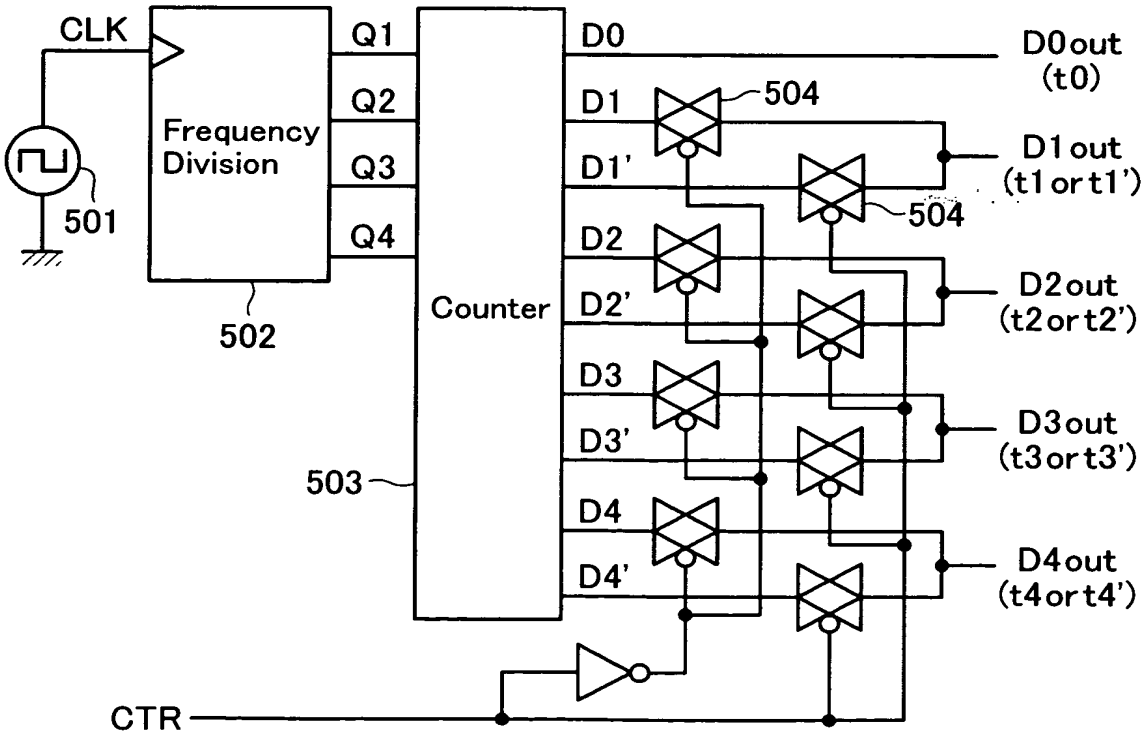

CLK
Q1
Q2
Q3
Q4
Frequency Division
501
502
Counter
503
D0
D1
D1'
D2
D2'
D3
D3'
D4
D4'
504
504
D0out (t0)
D1out (t1 or t1')
D2out (t2 or t2')
D3out (t3 or t3')
D4out (t4 or t4')
CTR

FIG. 7

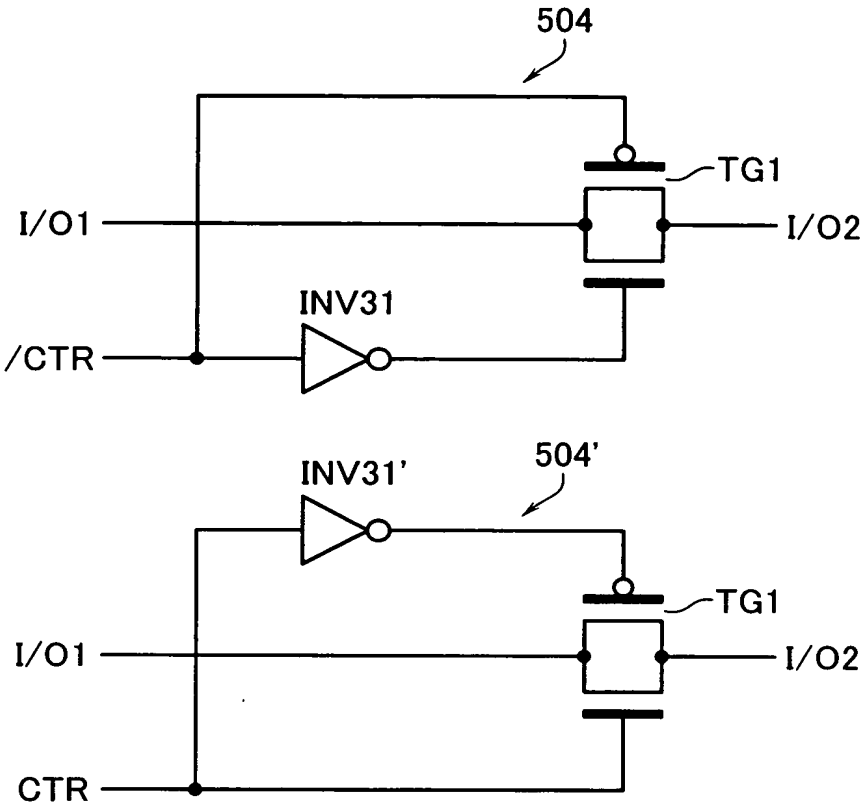

504
TG1
I/O1
I/O2
INV31
/CTR
INV31'
504'
TG1
I/O1
I/O2
CTR

FIG. 8

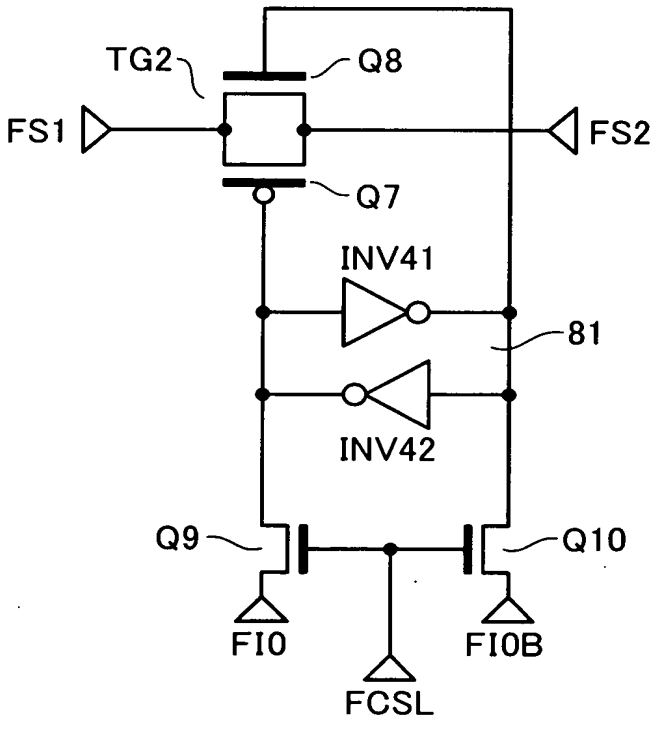

TG2
Q8
FS1
FS2
Q7
INV41
81
INV42
Q9
Q10
FI0
FI0B
FCSL

FIG. 9

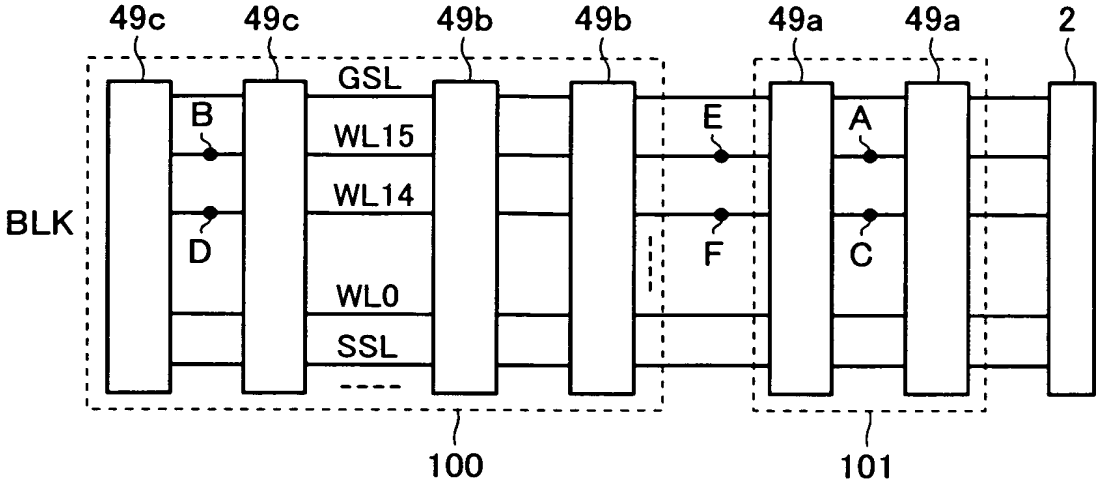


FIG. 10

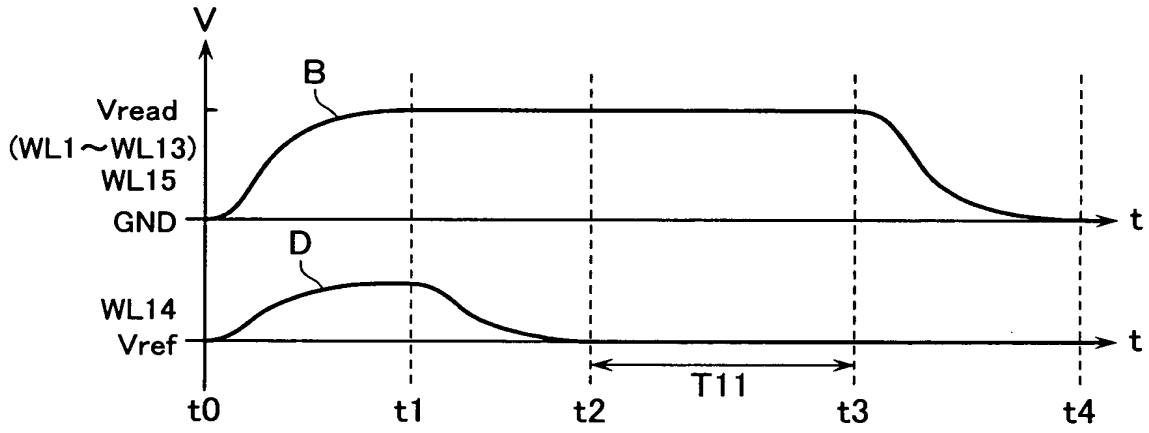


FIG. 11

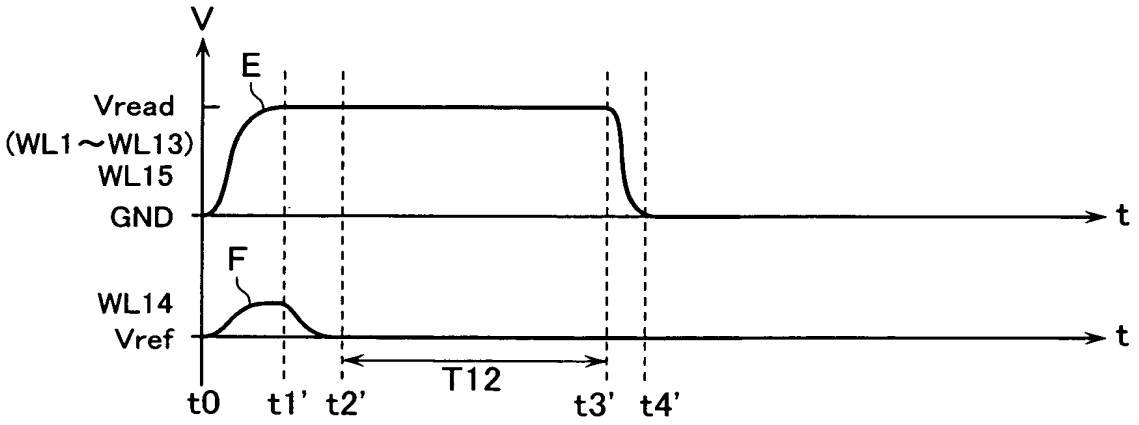


FIG. 12

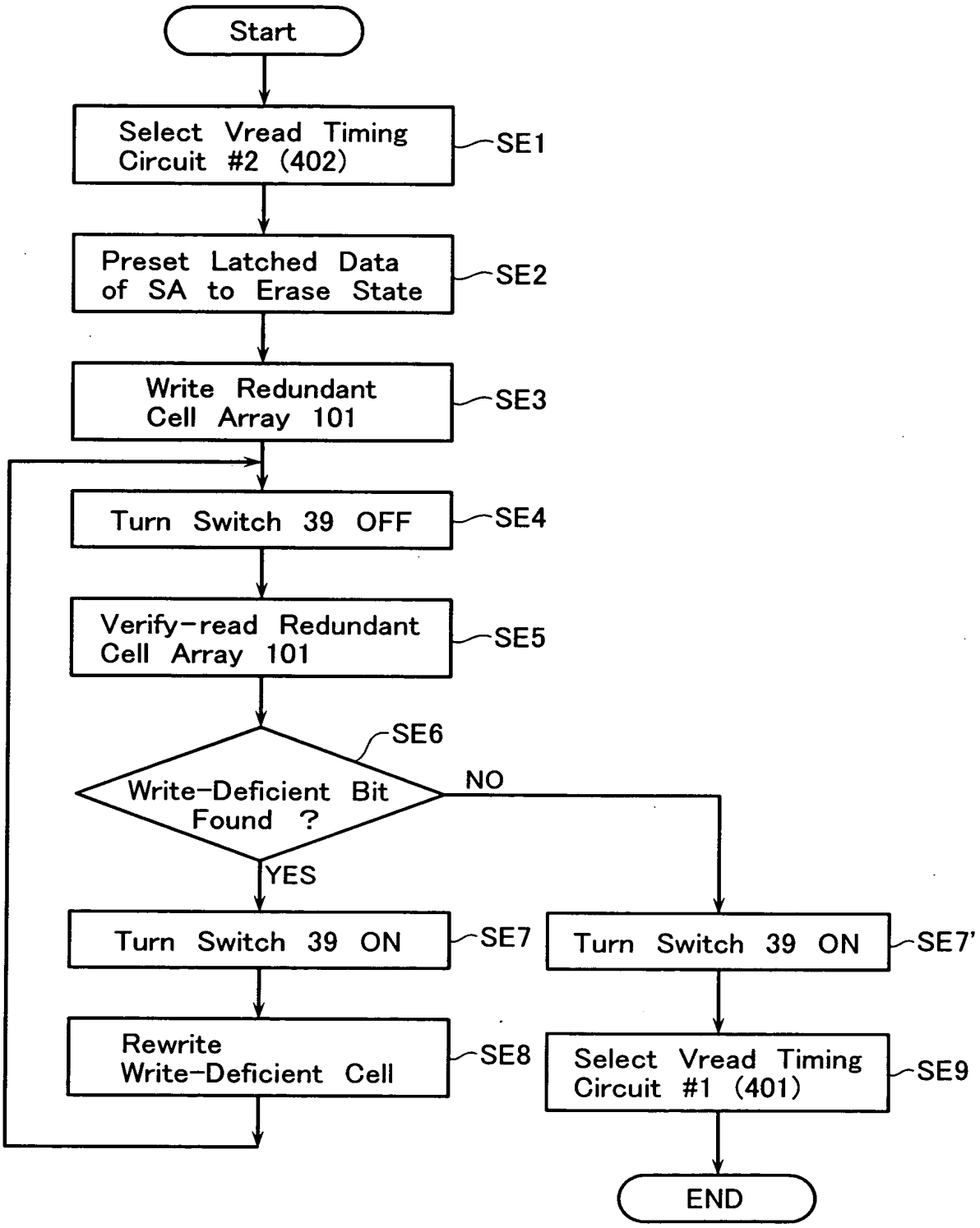

Start
Select Vread Timing Circuit #2 (402)
SE1
Preset Latched Data of SA to Erase State
SE2
Write Redundant Cell Array 101
SE3
Turn Switch 39 OFF
SE4
Verify-read Redundant Cell Array 101
SE5
SE6
Write-Deficient Bit Found ?
NO
YES
Turn Switch 39 ON
SE7
Rewrite Write-Deficient Cell
SE8
Turn Switch 39 ON
SE7'
Select Vread Timing Circuit #1 (401)
SE9
END

FIG. 13

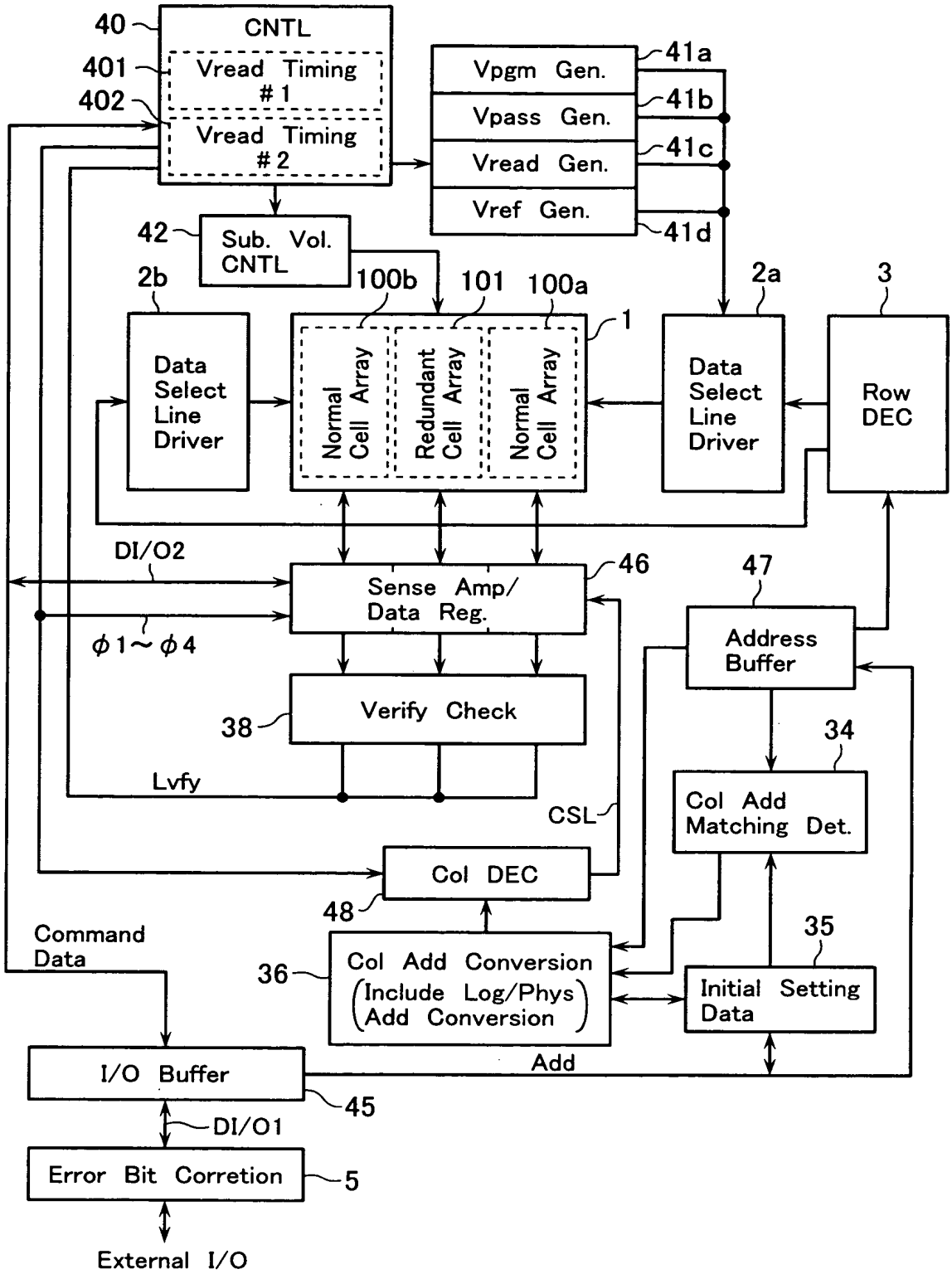

40
CNTL
401
Vread Timing #1
402
Vread Timing #2
Vpgm Gen.
Vpass Gen.
Vread Gen.
Vref Gen.
41a
41b
41c
41d
42
Sub. Vol. CNTL
2b
100b
101
100a
1
2a
3
Data Select Line Driver
Normal Cell Array
Redundant Cell Array
Normal Cell Array
Data Select Line Driver
Row DEC
DI/O2
Sense Amp/ Data Reg.
46
47
φ1～φ4
Address Buffer
38
Verify Check
34
Lvfy
CSL
Col Add Matching Det.
Col DEC
48
35
Command Data
36
Col Add Conversion (Include Log/Phys Add Conversion)
Initial Setting Data
Add
I/O Buffer
45
DI/O1
Error Bit Corretion
5
External I/O

FIG. 14A

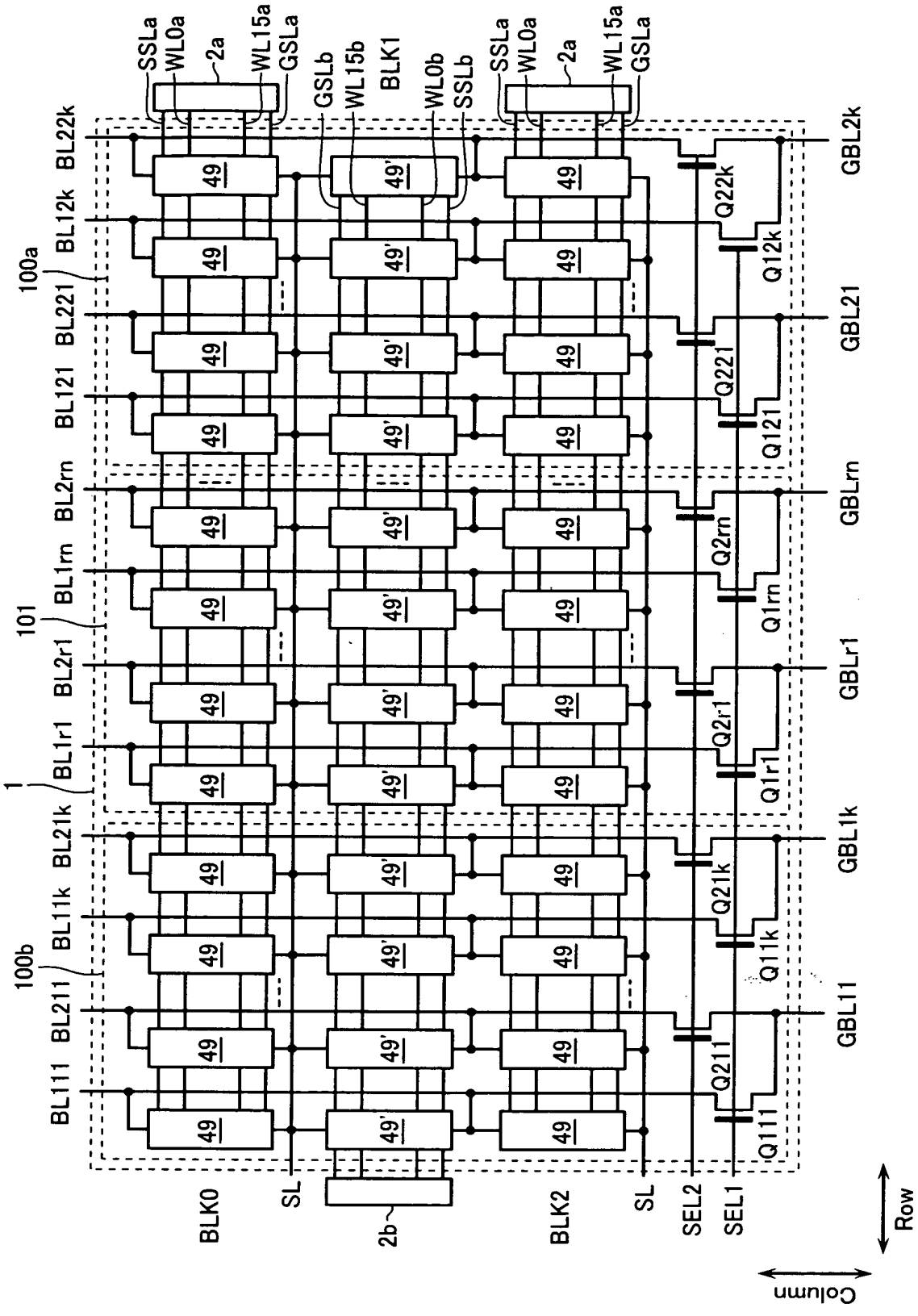

SSLa
WL0a
2a
WL15a
GSLa
GSLb
WL15b
BLK1
WL0b
SSLb
SSLa
WL0a
2a
WL15a
GSLa
BL22k
BL12k
BL221
BL121
BL2rn
BL1rn
BL2r1
BL1r1
BL21k
BL11k
BL211
BL111
100a
101
1
100b
49
49'
Q22k
Q12k
Q221
Q121
Q2rn
Q1rn
Q2r1
Q1r1
Q21k
Q11k
Q211
Q111
GBL2k
GBL21
GBLrn
GBLr1
GBL1k
GBL11
BLK0
SL
2b
BLK2
SL
SEL2
SEL1
Column
Row

FIG. 14B

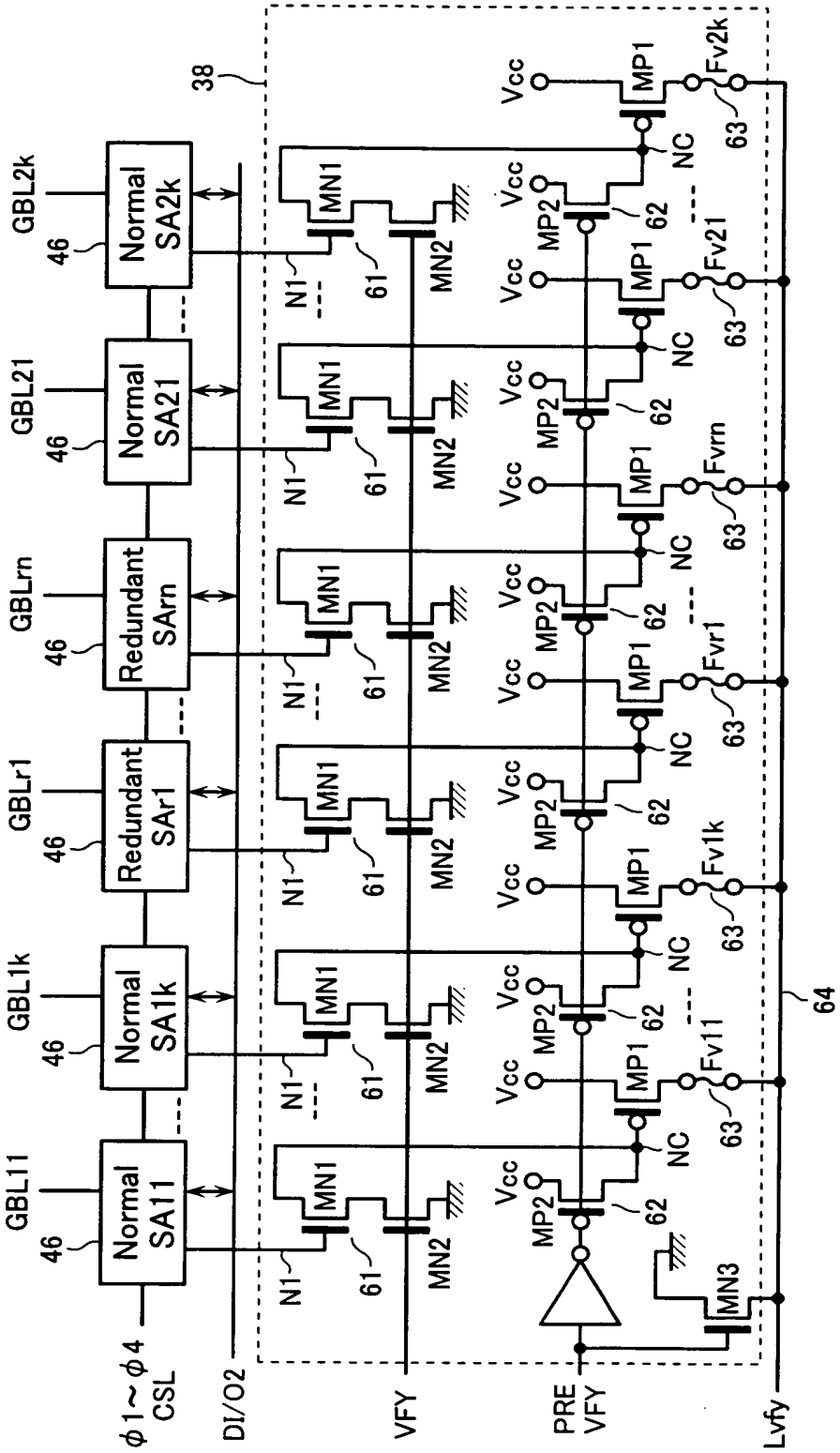

38
GBL11
GBL1k
GBLr1
GBLrn
GBL21
GBL2k
46
Normal SA11
Normal SA1k
Redundant SAr1
Redundant SArn
Normal SA21
Normal SA2k
φ1~φ4
CSL
DI/O2
VFY
PRE
VFY
Lvfy
64
N1
MN1
MN2
MN3
61
62
63
MP1
MP2
Vcc
NC
Fv11
Fv1k
Fvr1
Fvrn
Fv21
Fv2k

FIG. 15

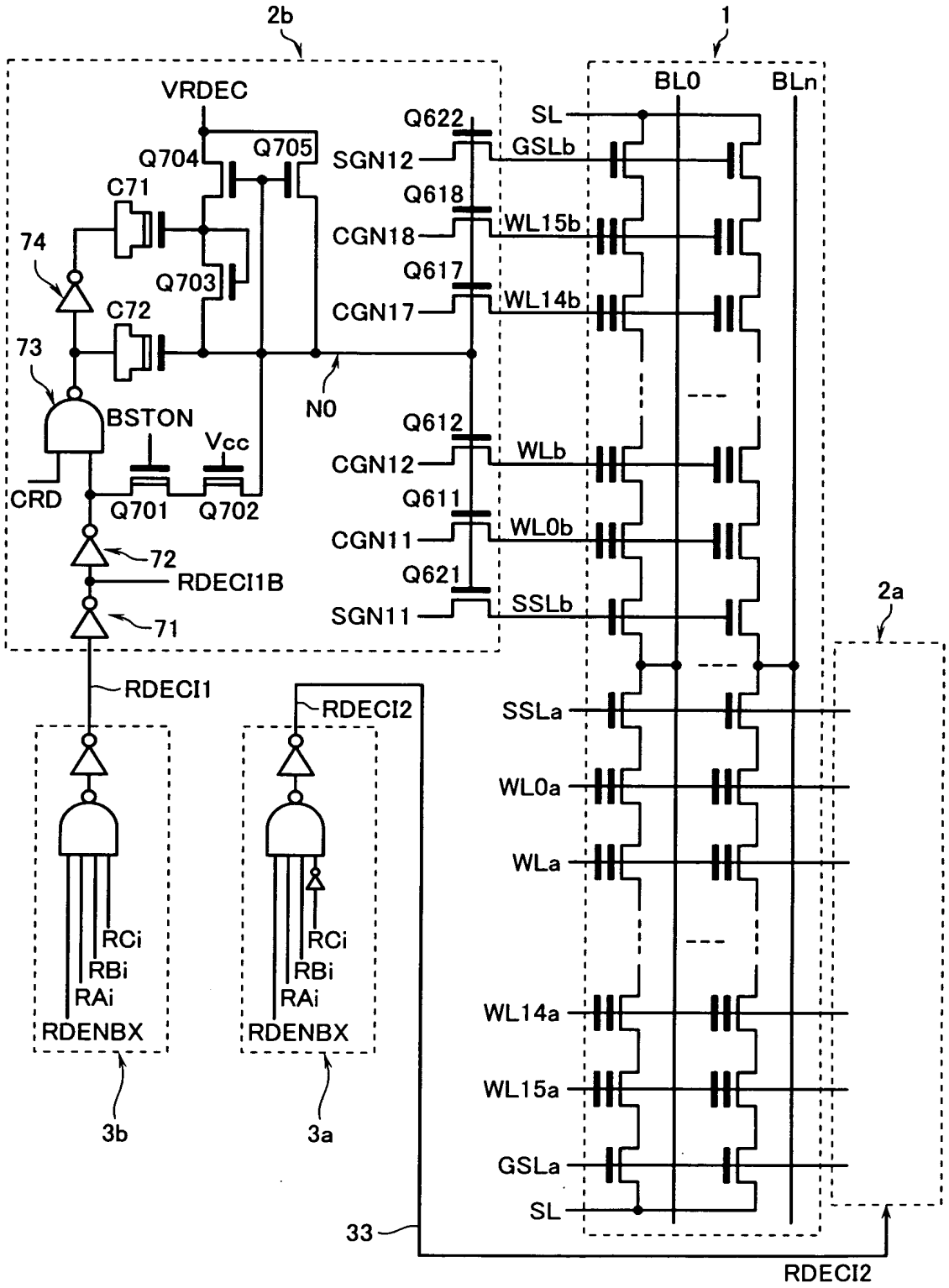

2b
1
VRDEC
BL0
BLn
Q622
SL
GSLb
Q704
Q705
SGN12
C71
Q618
CGN18
WL15b
74
Q703
Q617
CGN17
WL14b
C72
73
N0
BSTON
Vcc
Q612
CGN12
WLb
CRD
Q701
Q702
Q611
CGN11
WL0b
72
RDECI1B
Q621
SGN11
SSLb
2a
71
RDECI1
RDECI2
SSLa
WL0a
WLa
RCi
RBi
RAi
RDENBX
WL14a
WL15a
GSLa
SL
33
3b
3a
RDECI2

FIG. 16

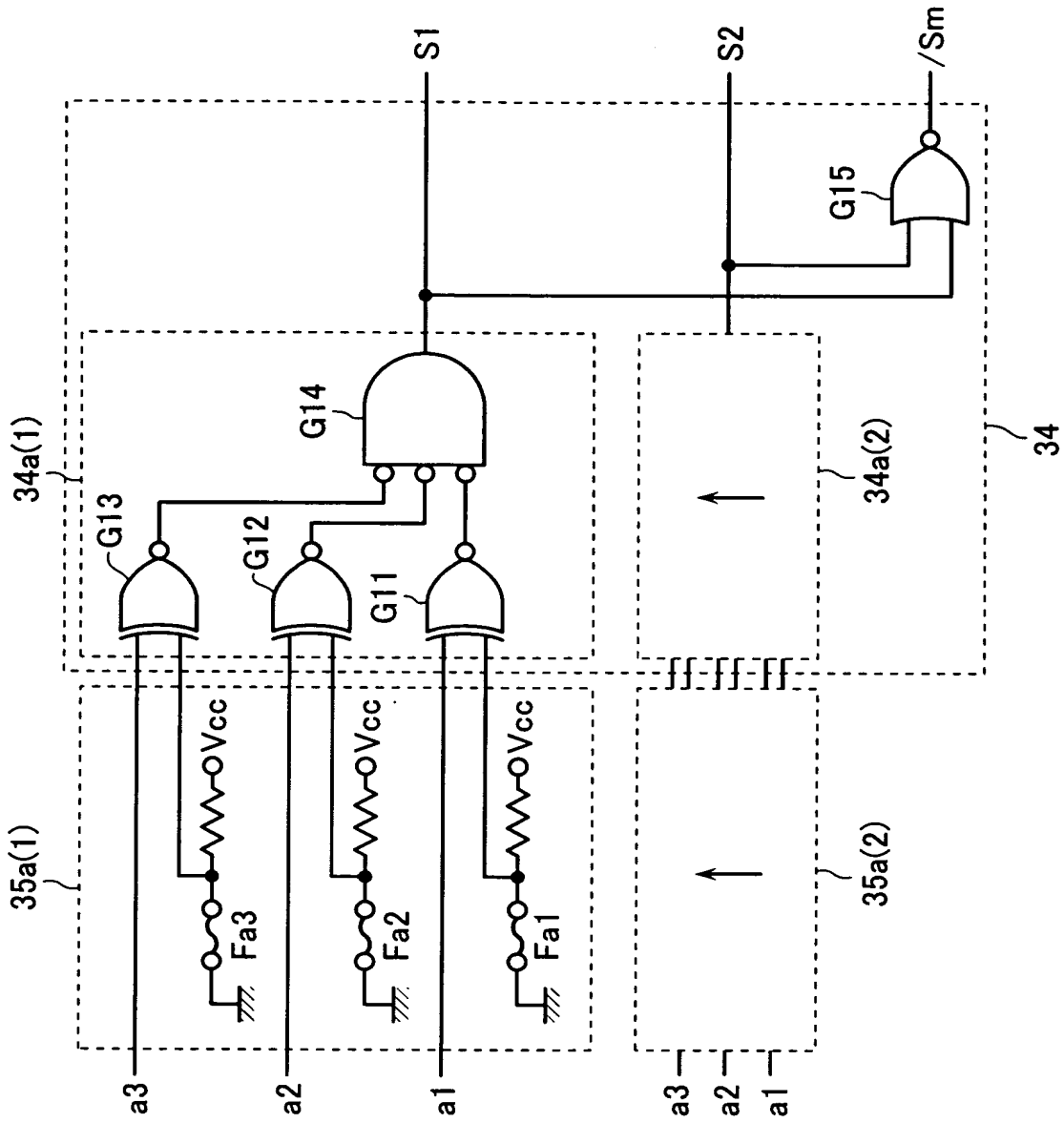

S1
S2
/Sm
G15
G14
G13
G12
G11
34a(1)
34a(2)
34
35a(1)
35a(2)
Vcc
Fa3
Fa2
Fa1
a3
a2
a1
a3
a2
a1

FIG. 17

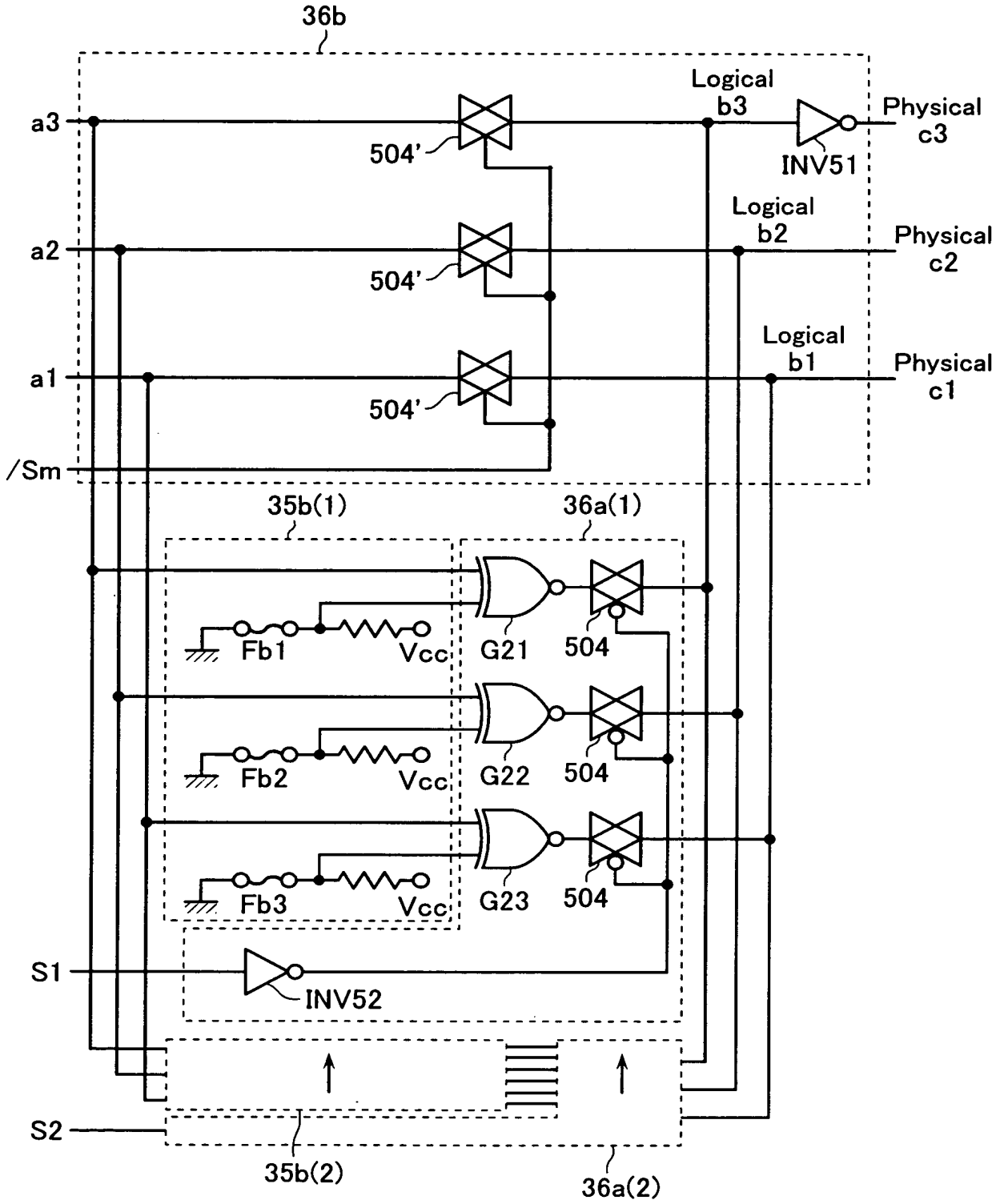

36b
a3
a2
a1
/Sm
504'
504'
504'
Logical b3
Logical b2
Logical b1
Physical c3
Physical c2
Physical c1
INV51
35b(1)
36a(1)
Fb1
Vcc
G21
504
Fb2
Vcc
G22
504
Fb3
Vcc
G23
504
S1
INV52
S2
35b(2)
36a(2)

FIG. 18

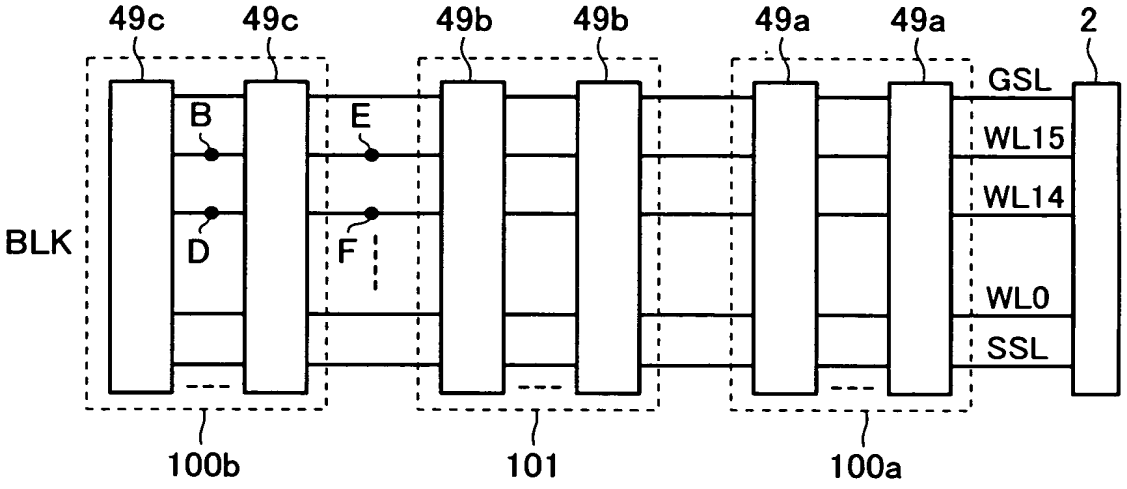


FIG. 19

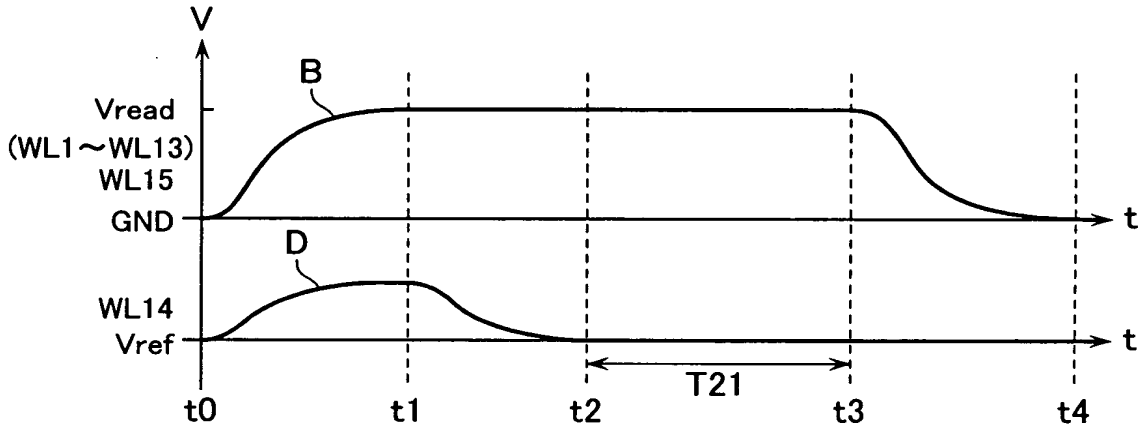


FIG. 20

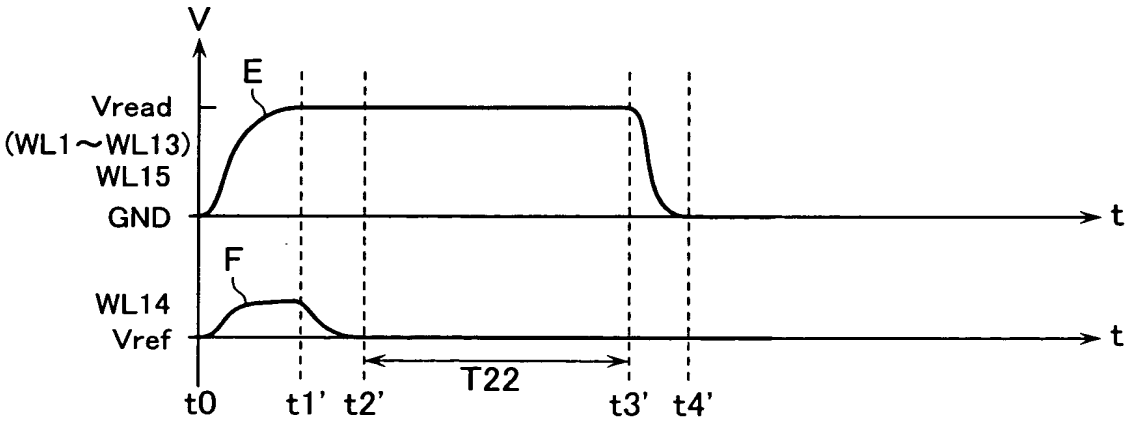


FIG. 21

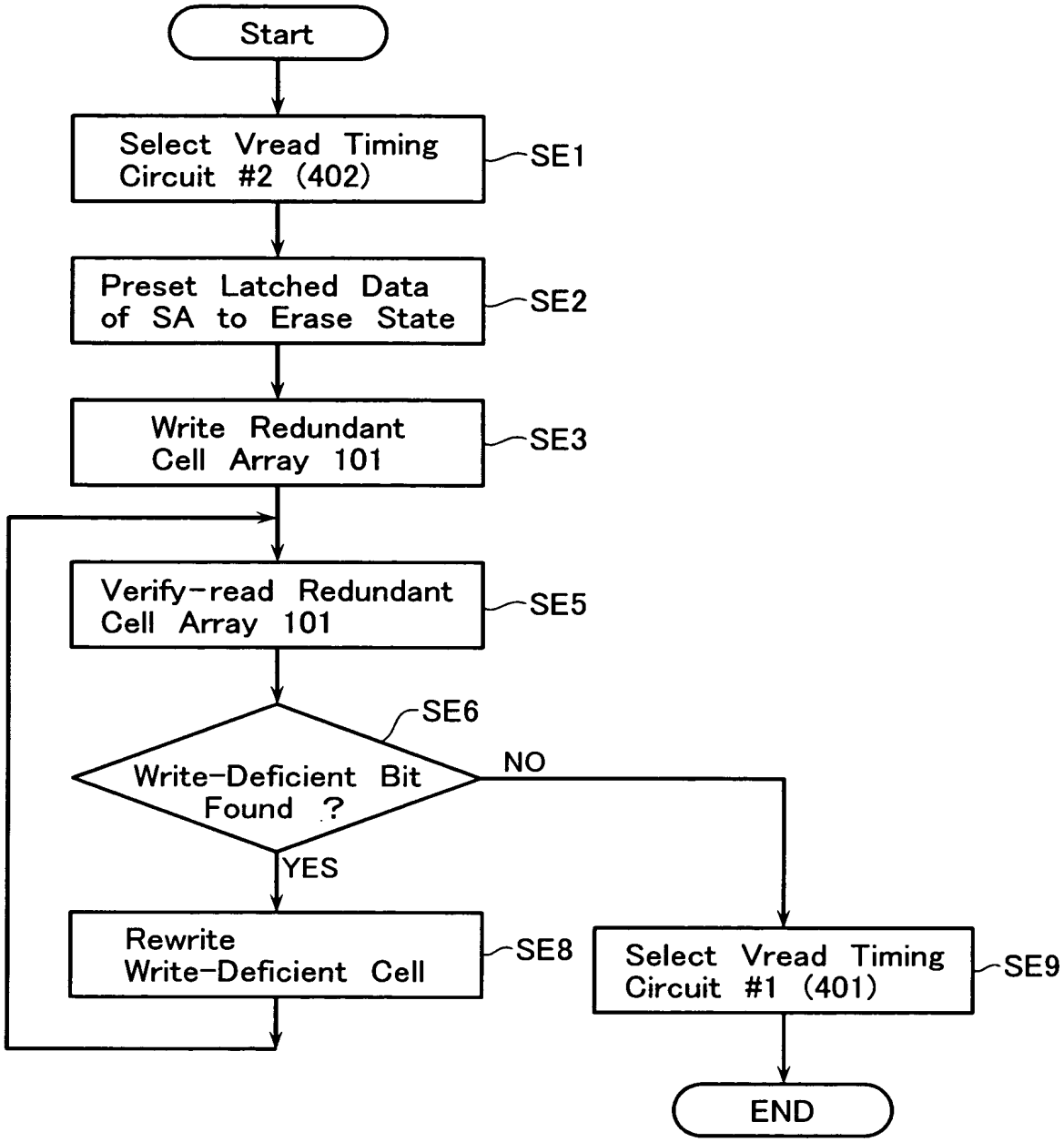

Start
Select Vread Timing Circuit #2 (402)
SE1
Preset Latched Data of SA to Erase State
SE2
Write Redundant Cell Array 101
SE3
Verify-read Redundant Cell Array 101
SE5
SE6
Write-Deficient Bit Found ?
NO
YES
Rewrite Write-Deficient Cell
SE8
Select Vread Timing Circuit #1 (401)
SE9
END

FIG. 22

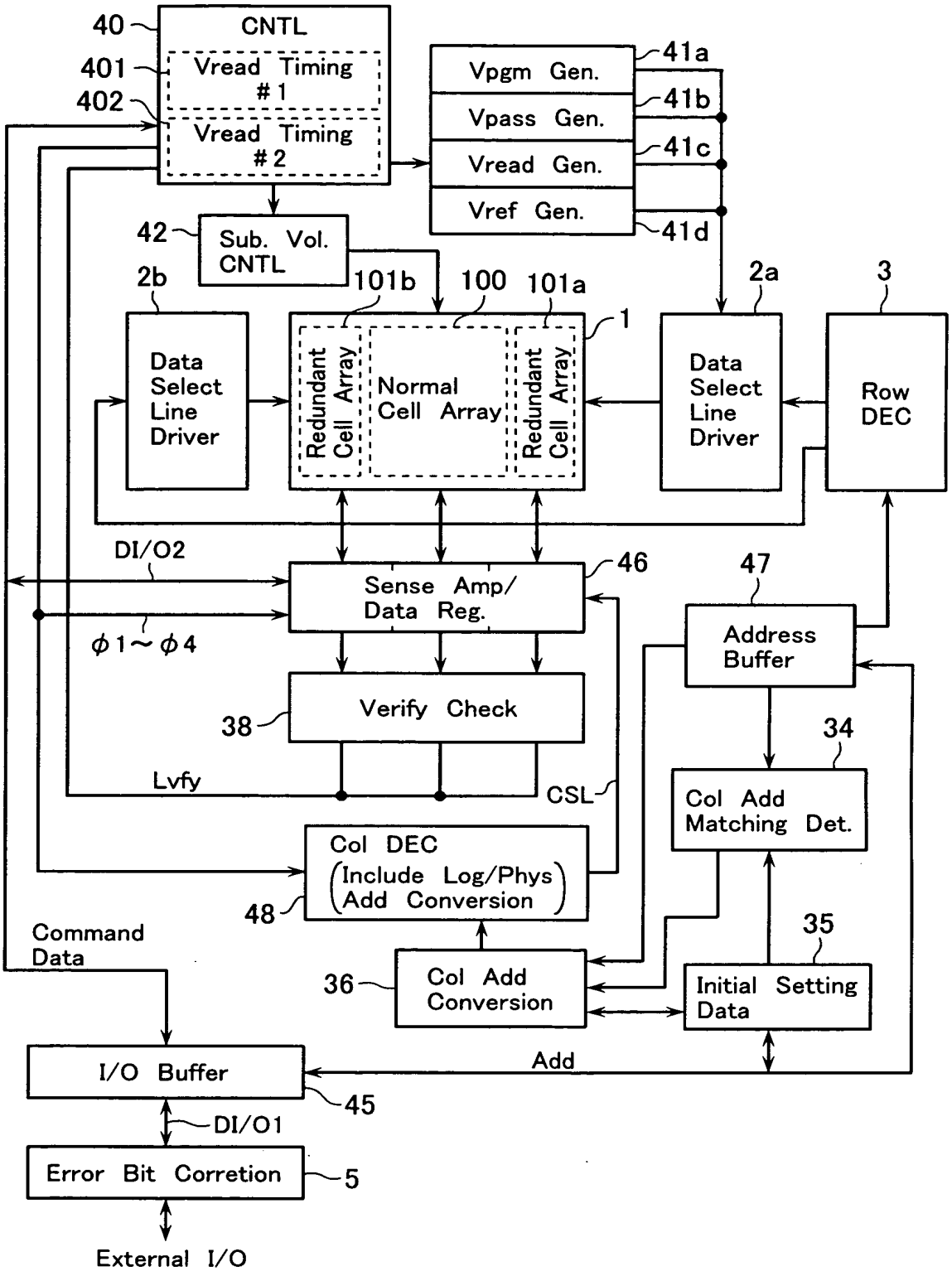

40
CNTL
401
Vread Timing #1
402
Vread Timing #2
Vpgm Gen.
Vpass Gen.
Vread Gen.
Vref Gen.
41a
41b
41c
41d
42
Sub. Vol. CNTL
2b
101b
100
101a
1
2a
3
Data Select Line Driver
Redundant Cell Array
Normal Cell Array
Redundant Cell Array
Data Select Line Driver
Row DEC
DI/O2
Sense Amp/ Data Reg.
46
47
φ1～φ4
Address Buffer
Verify Check
38
34
Lvfy
CSL
Col Add Matching Det.
Col DEC (Include Log/Phys Add Conversion)
48
Command Data
35
36
Col Add Conversion
Initial Setting Data
Add
I/O Buffer
45
DI/O1
Error Bit Corretion
5
External I/O

FIG. 23A

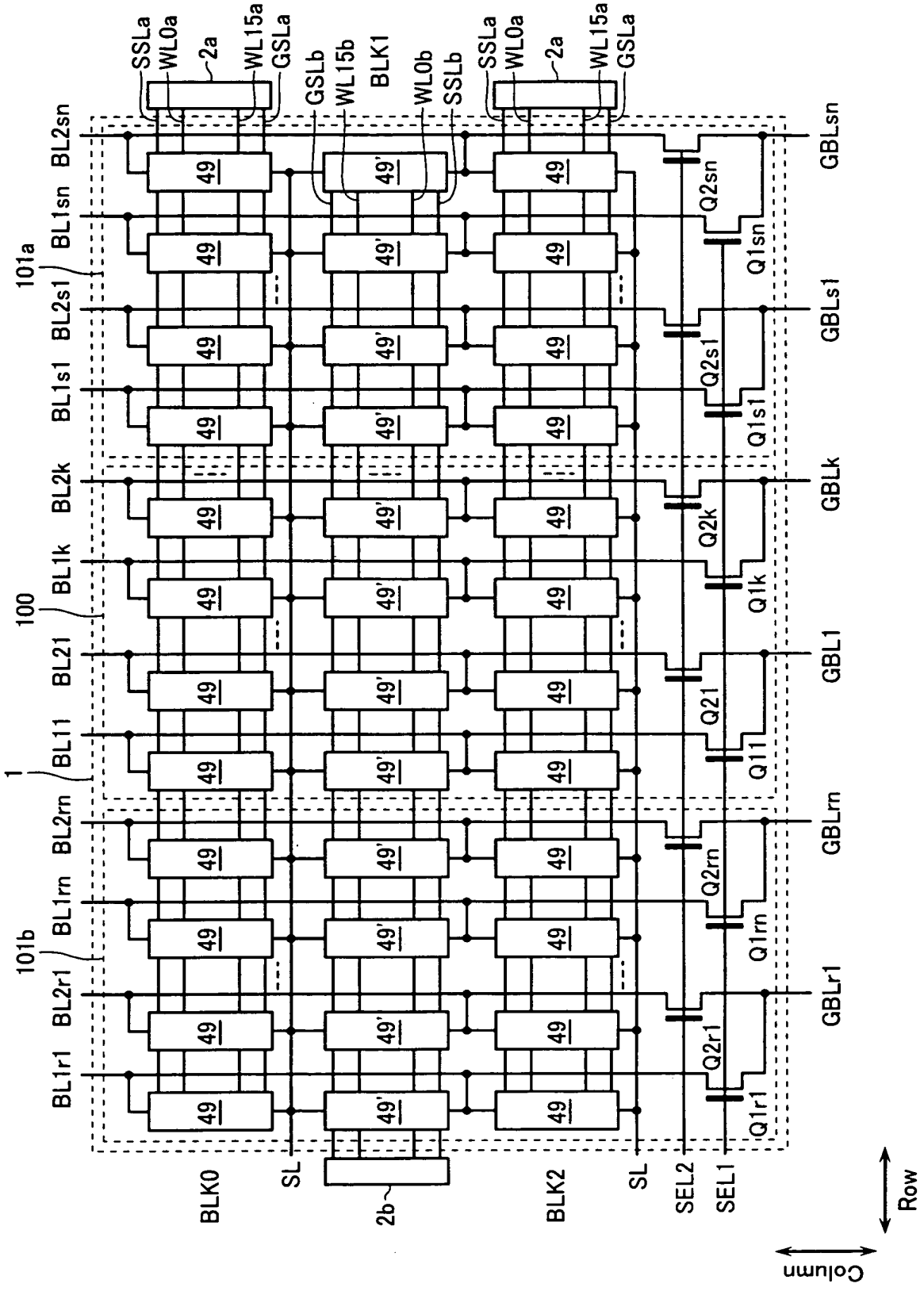

SSLa
WL0a
2a
WL15a
GSLa
GSLb
WL15b
BLK1
WL0b
SSLb
BL2sn
BL1sn
BL2s1
BL1s1
BL2k
BL1k
BL21
BL11
BL2rn
BL1rn
BL2r1
BL1r1
101a
100
1
101b
49
49'
Q2sn
Q1sn
Q2s1
Q1s1
Q2k
Q1k
Q21
Q11
Q2rn
Q1rn
Q2r1
Q1r1
GBLsn
GBLs1
GBLk
GBL1
GBLrn
GBLr1
BLK0
SL
2b
BLK2
SL
SEL2
SEL1
Column
Row

FIG. 23B

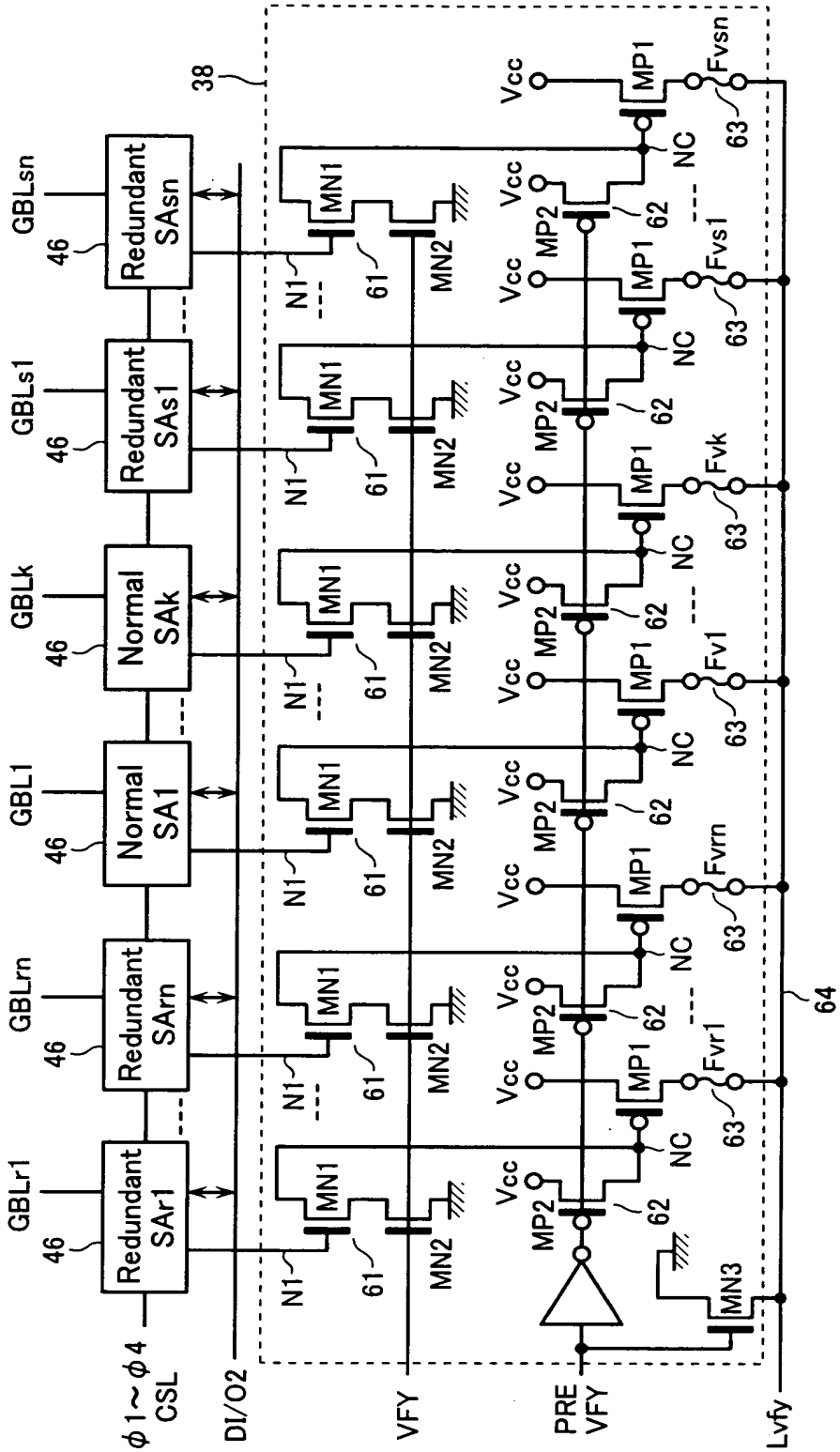

Redundant SAr1
Redundant SArn
Normal SA1
Normal SAk
Redundant SAs1
Redundant SAsn
GBLr1
GBLrn
GBL1
GBLk
GBLs1
GBLsn
46
φ1~φ4
CSL
DI/O2
VFY
PRE
VFY
Lvfy
38
64
MN1
MN2
MN3
MP1
MP2
N1
61
62
63
NC
Vcc
Fvr1
Fvrn
Fv1
Fvk
Fvs1
Fvsn

FIG. 24

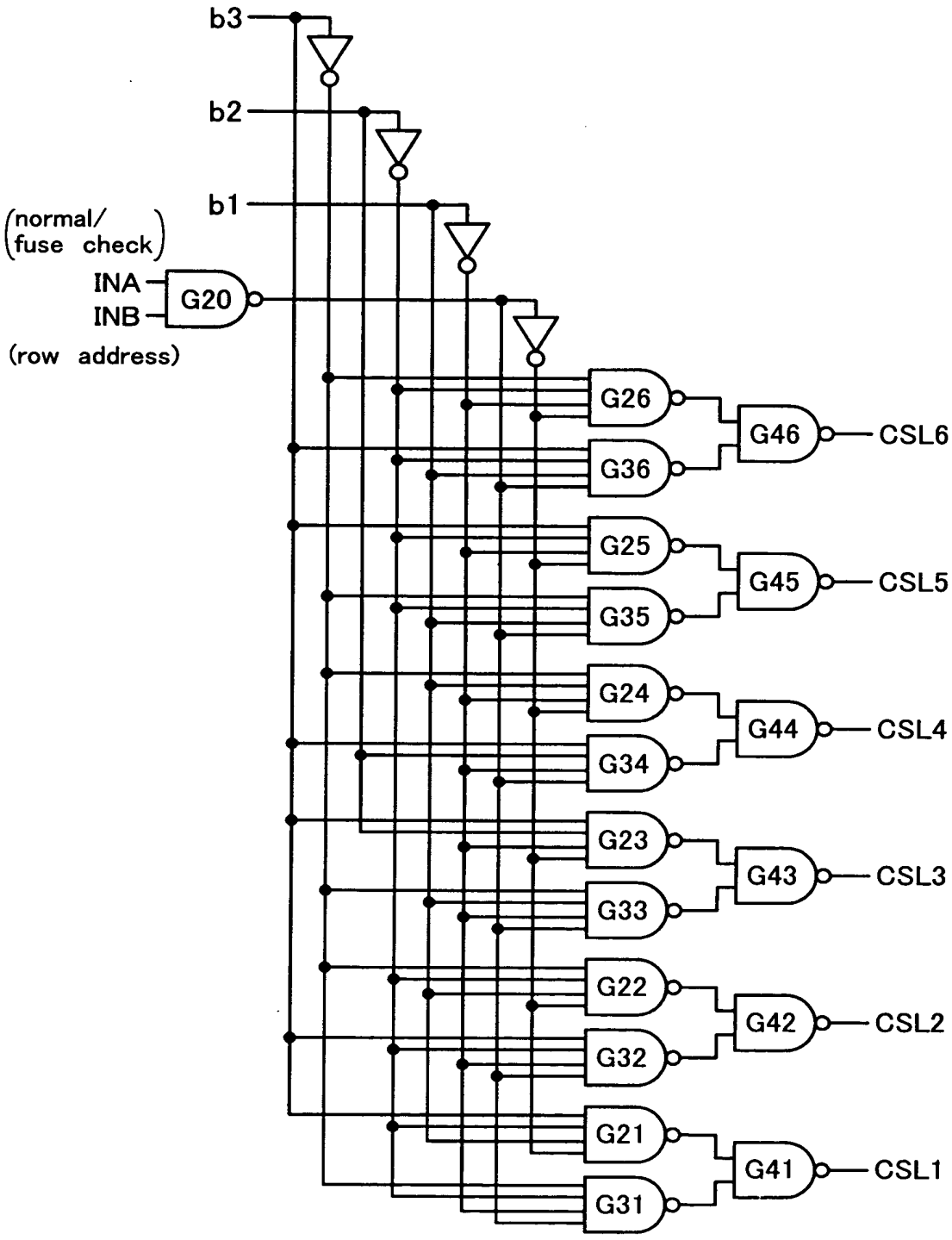

b3
b2
b1
(normal/
fuse check)
INA
INB
G20
(row address)
G26
G36
G46
CSL6
G25
G35
G45
CSL5
G24
G34
G44
CSL4
G23
G33
G43
CSL3
G22
G32
G42
CSL2
G21
G31
G41
CSL1

FIG. 25

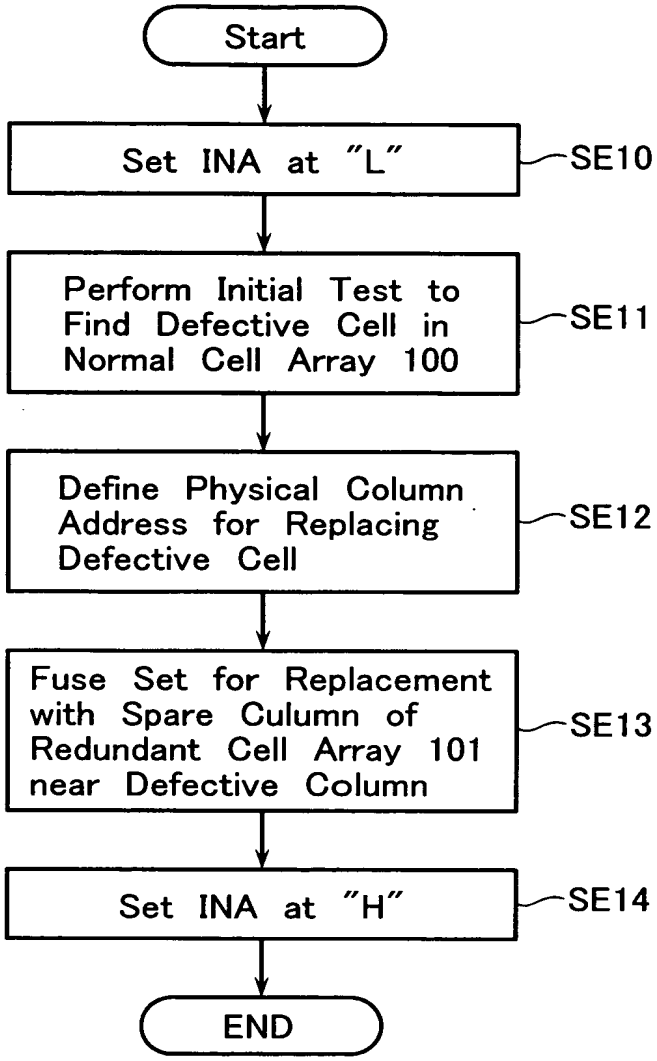

Start
Set INA at "L"
SE10
Perform Initial Test to Find Defective Cell in Normal Cell Array 100
SE11
Define Physical Column Address for Replacing Defective Cell
SE12
Fuse Set for Replacement with Spare Culumn of Redundant Cell Array 101 near Defective Column
SE13
Set INA at "H"
SE14
END

FIG. 26

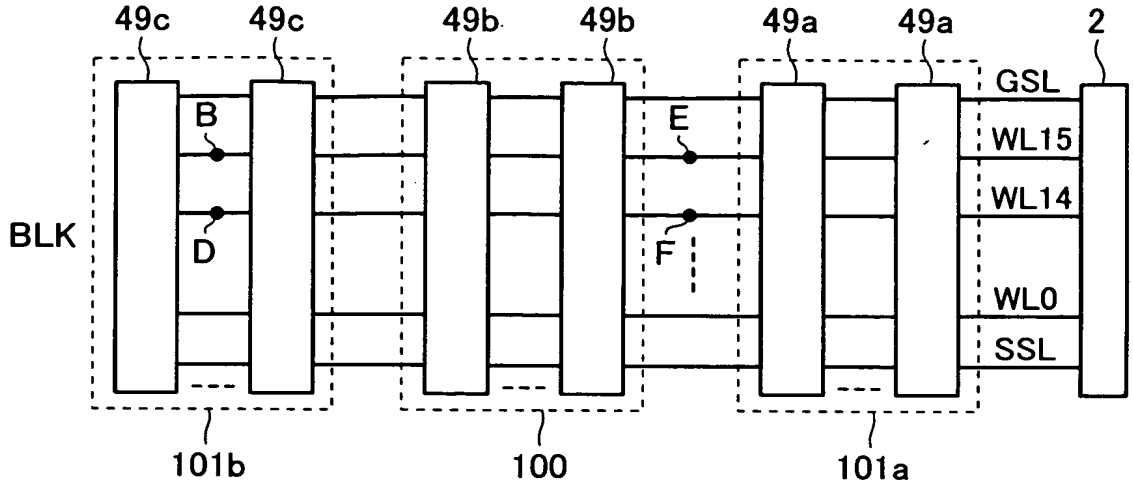


FIG. 27

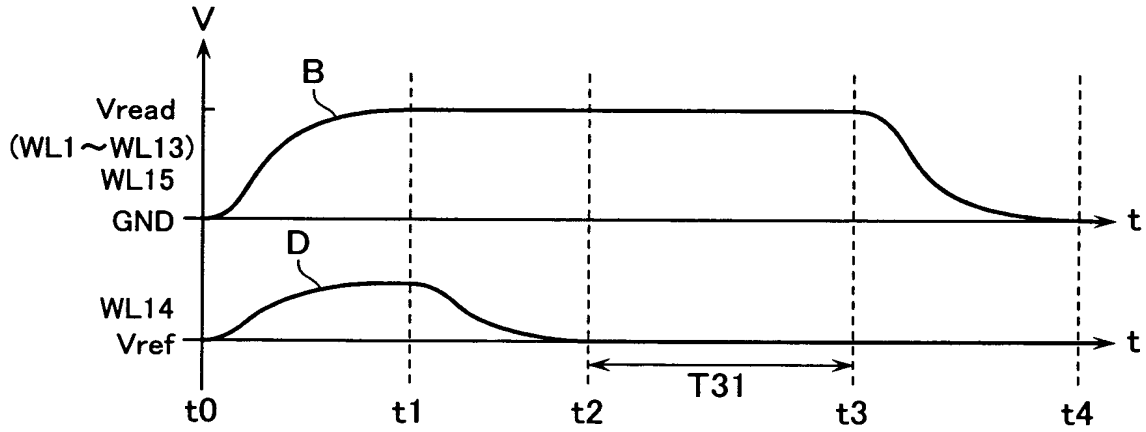


FIG. 28

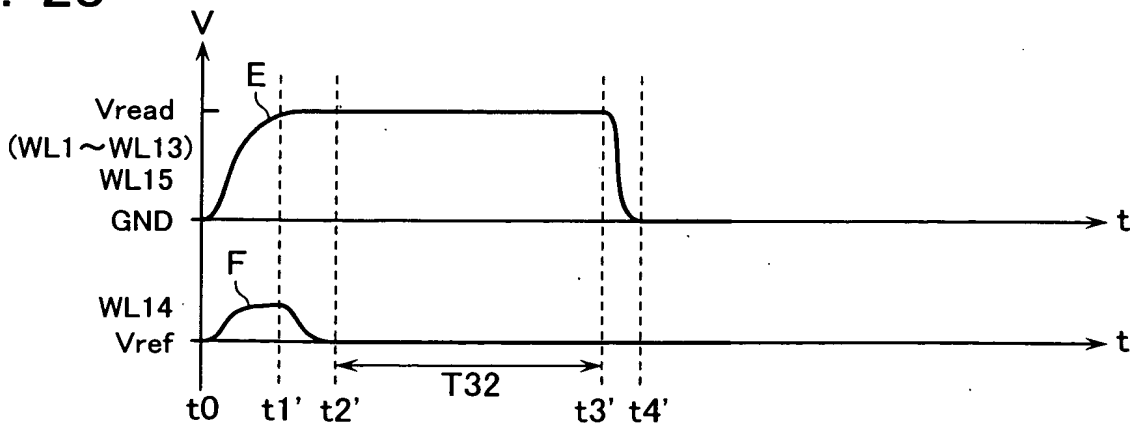


FIG. 29

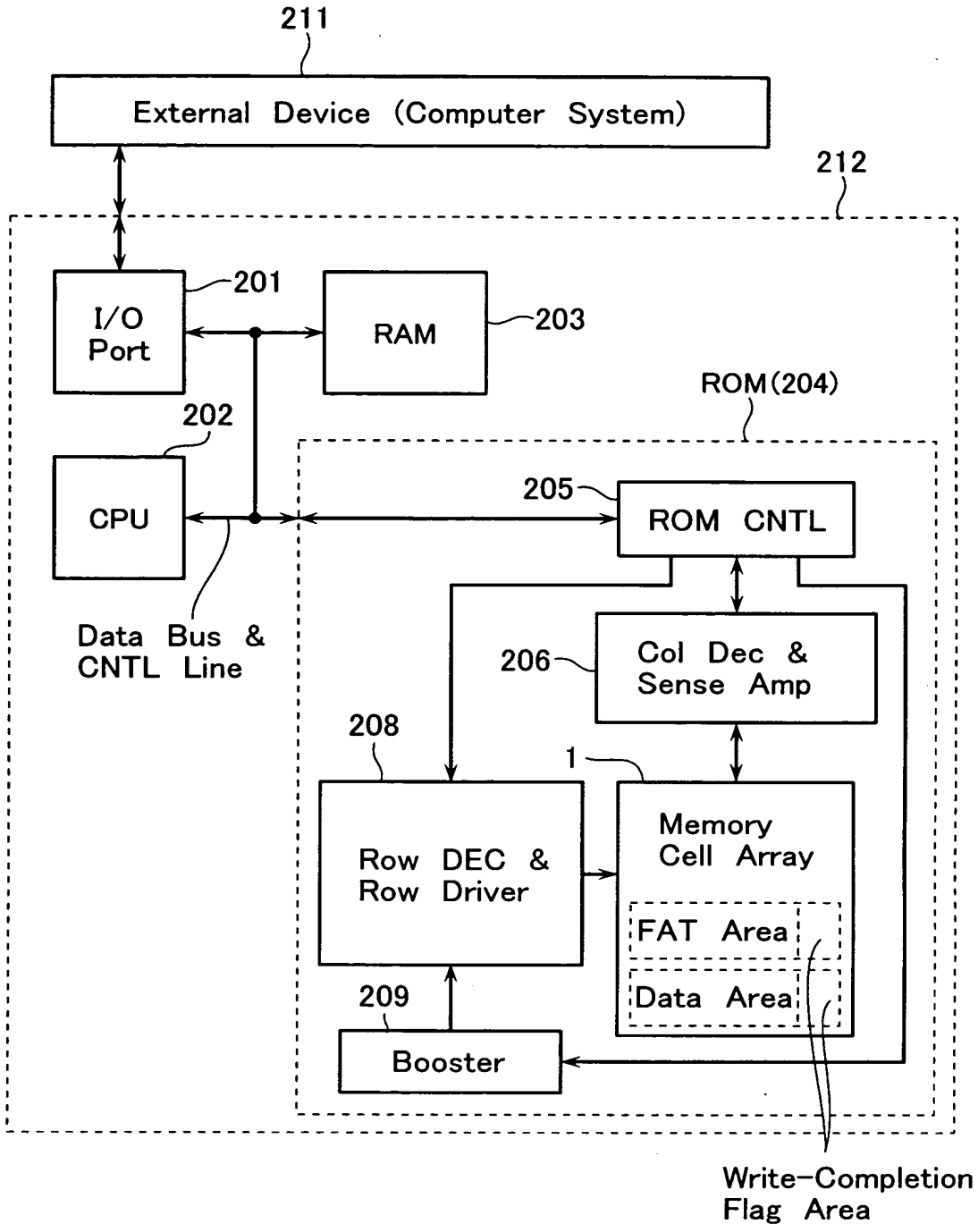

211
External Device (Computer System)
212
201
I/O Port
RAM
203
ROM(204)
202
CPU
205
ROM CNTL
Data Bus & CNTL Line
206
Col Dec & Sense Amp
208
1
Row DEC & Row Driver
Memory Cell Array
FAT Area
Data Area
209
Booster
Write-Completion Flag Area

FIG. 30

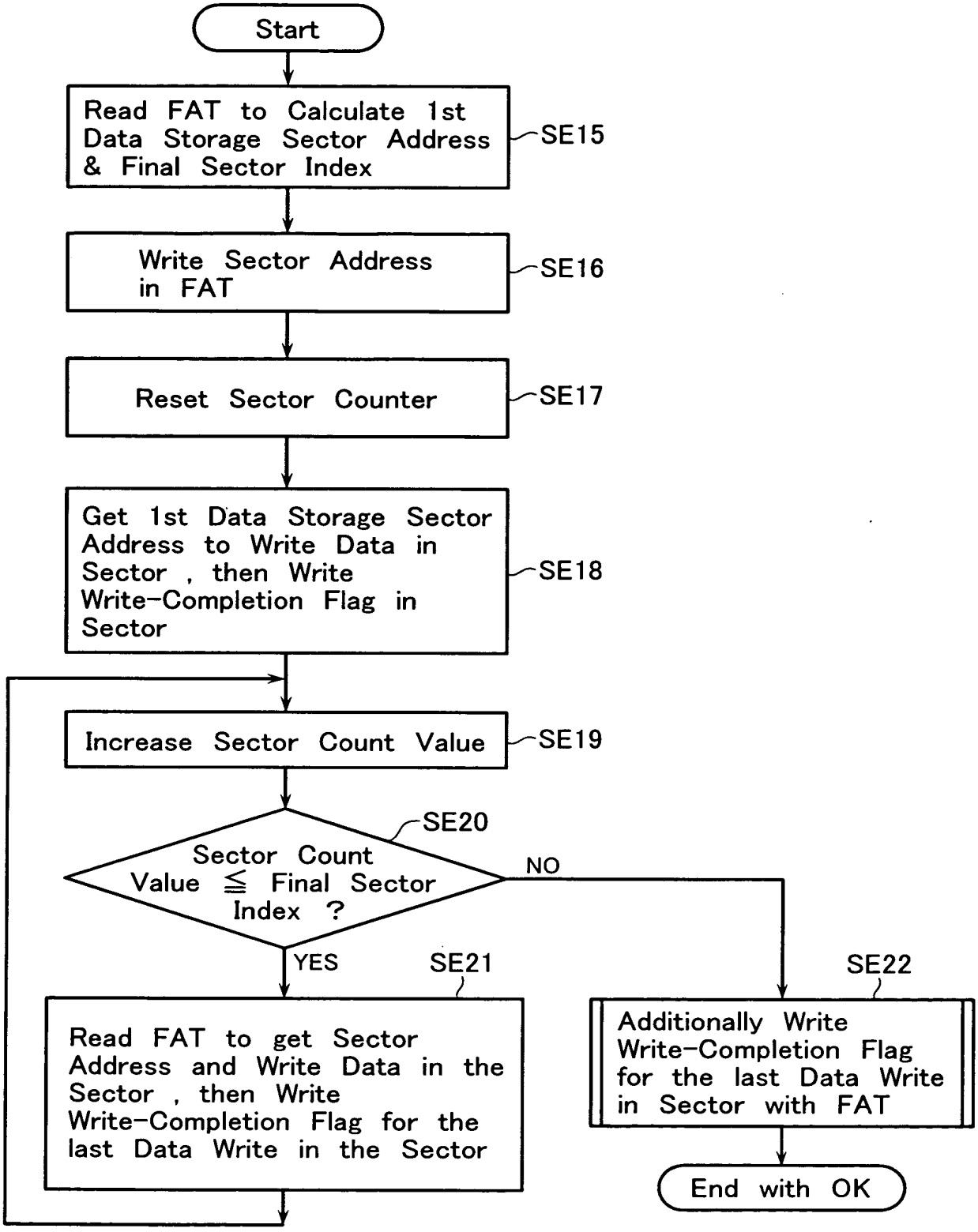

Start
Read FAT to Calculate 1st Data Storage Sector Address & Final Sector Index
SE15
Write Sector Address in FAT
SE16
Reset Sector Counter
SE17
Get 1st Data Storage Sector Address to Write Data in Sector , then Write Write-Completion Flag in Sector
SE18
Increase Sector Count Value
SE19
SE20
Sector Count Value ≦ Final Sector Index ?
NO
YES
SE21
Read FAT to get Sector Address and Write Data in the Sector , then Write Write-Completion Flag for the last Data Write in the Sector
SE22
Additionally Write Write-Completion Flag for the last Data Write in Sector with FAT
End with OK

FIG. 31

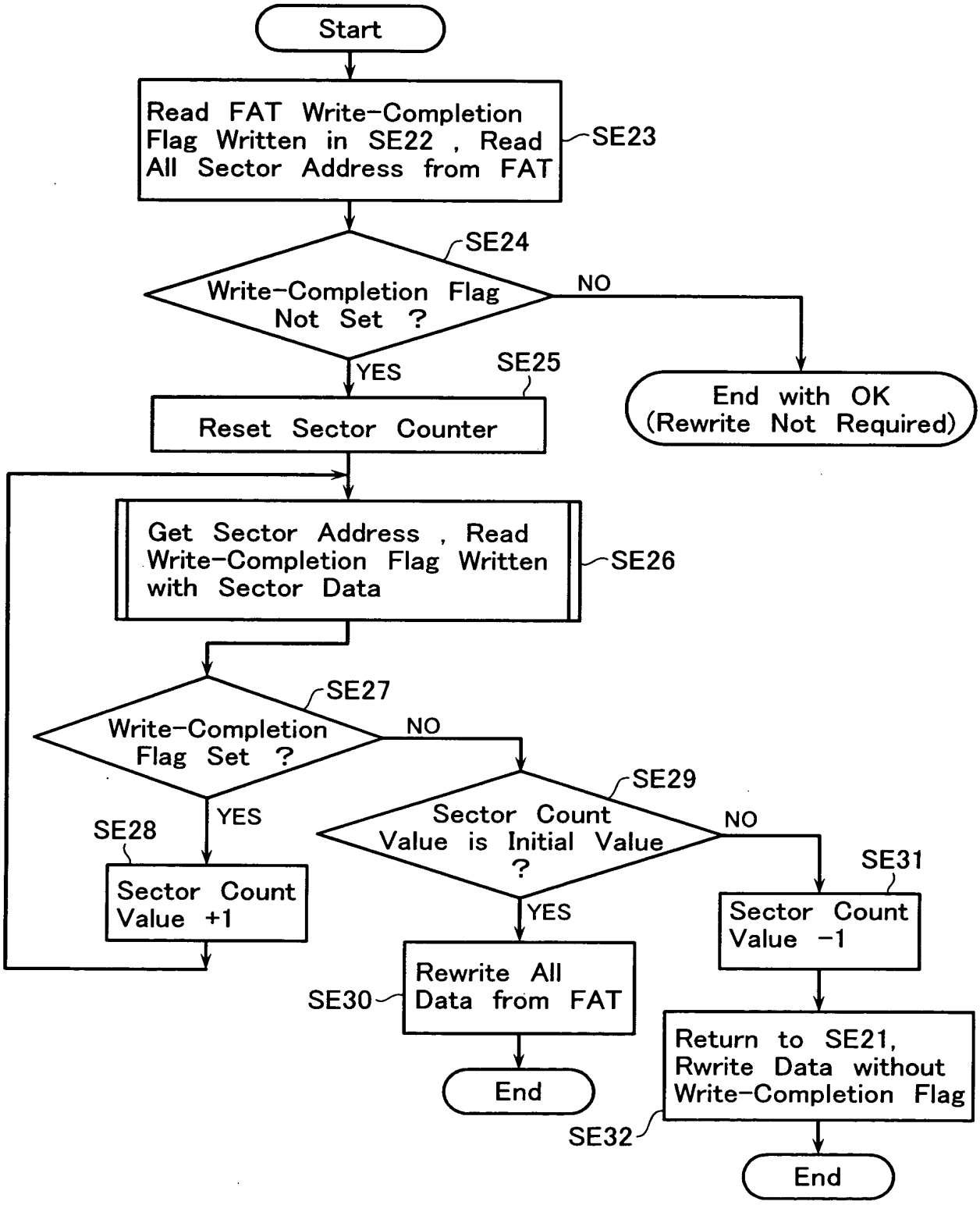

Start
Read FAT Write-Completion Flag Written in SE22 , Read All Sector Address from FAT
SE23
SE24
Write-Completion Flag Not Set ?
NO
YES
SE25
End with OK (Rewrite Not Required)
Reset Sector Counter
Get Sector Address , Read Write-Completion Flag Written with Sector Data
SE26
SE27
Write-Completion Flag Set ?
NO
YES
SE28
SE29
Sector Count Value is Initial Value ?
NO
YES
SE31
Sector Count Value +1
Sector Count Value -1
SE30
Rewrite All Data from FAT
Return to SE21, Rwrite Data without Write-Completion Flag
SE32
End
End

FIG. 32

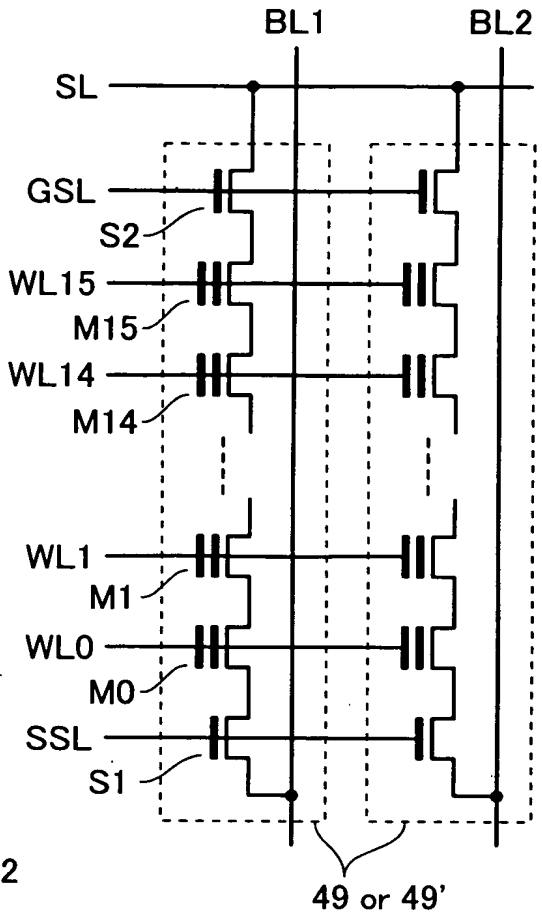

BL1
BL2
SL
GSL
S2
WL15
M15
WL14
M14
WL1
M1
WL0
M0
SSL
S1
49 or 49'

FIG. 33

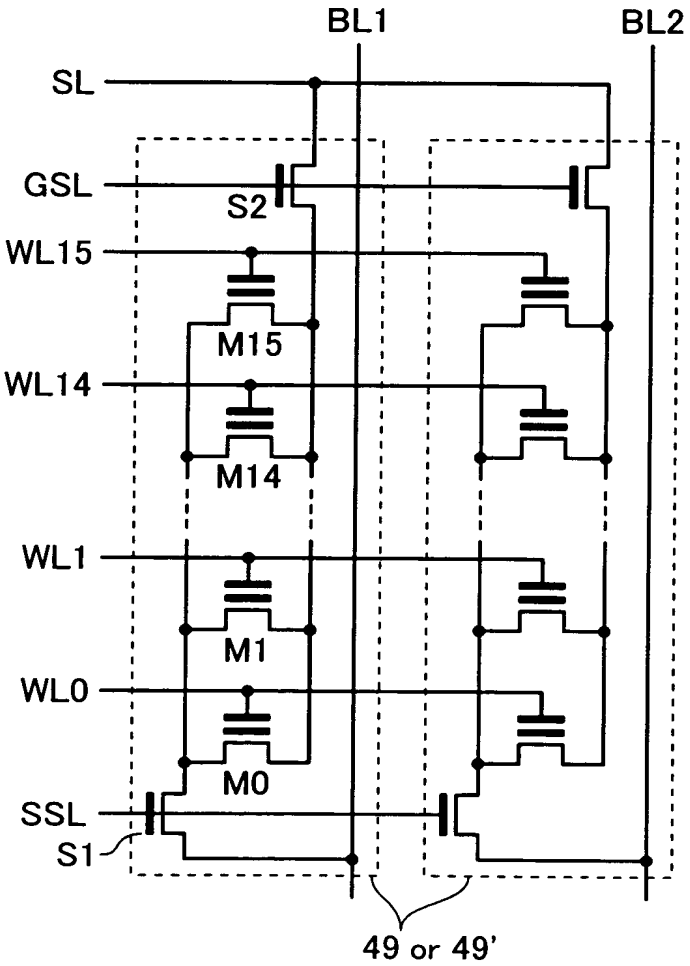

BL1
BL2
SL
GSL
S2
WL15
M15
WL14
M14
WL1
M1
WL0
M0
SSL
S1
49 or 49'

FIG. 34

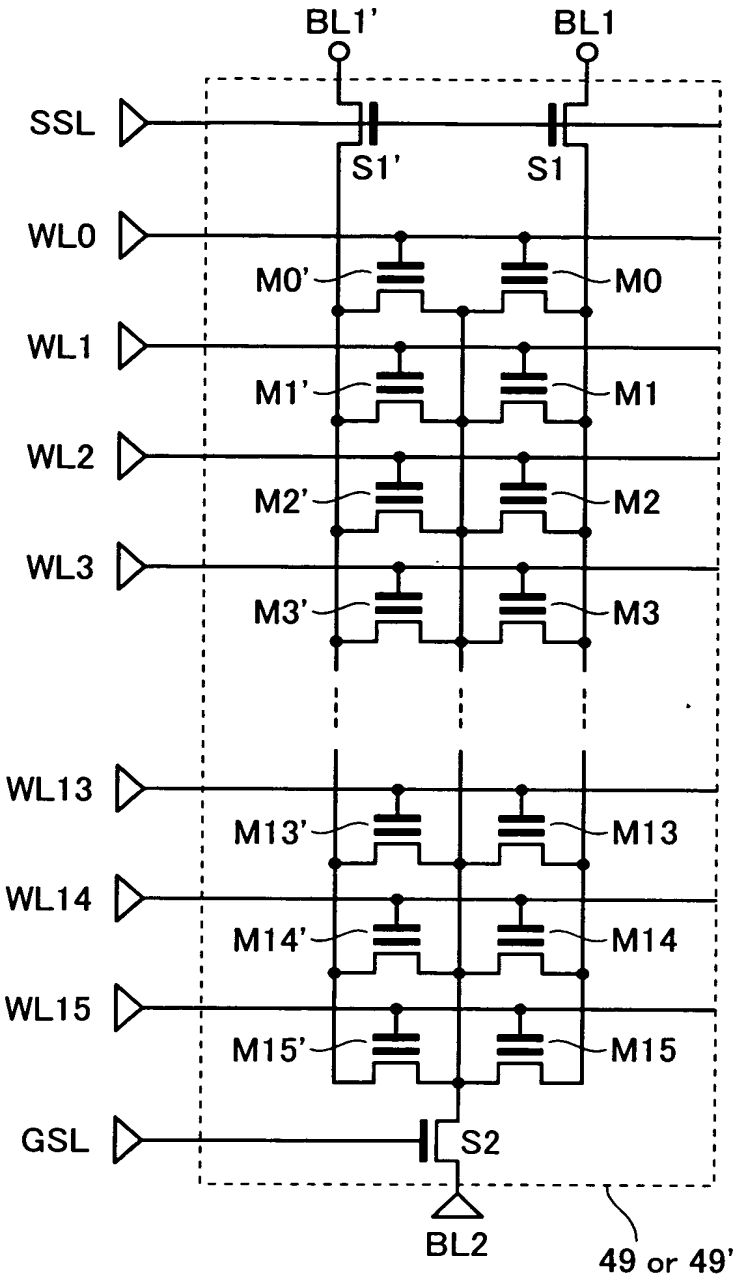

BL1'
BL1
SSL
S1'
S1
WL0
M0'
M0
WL1
M1'
M1
WL2
M2'
M2
WL3
M3'
M3
WL13
M13'
M13
WL14
M14'
M14
WL15
M15'
M15
GSL
S2
BL2
49 or 49'

FIG. 35

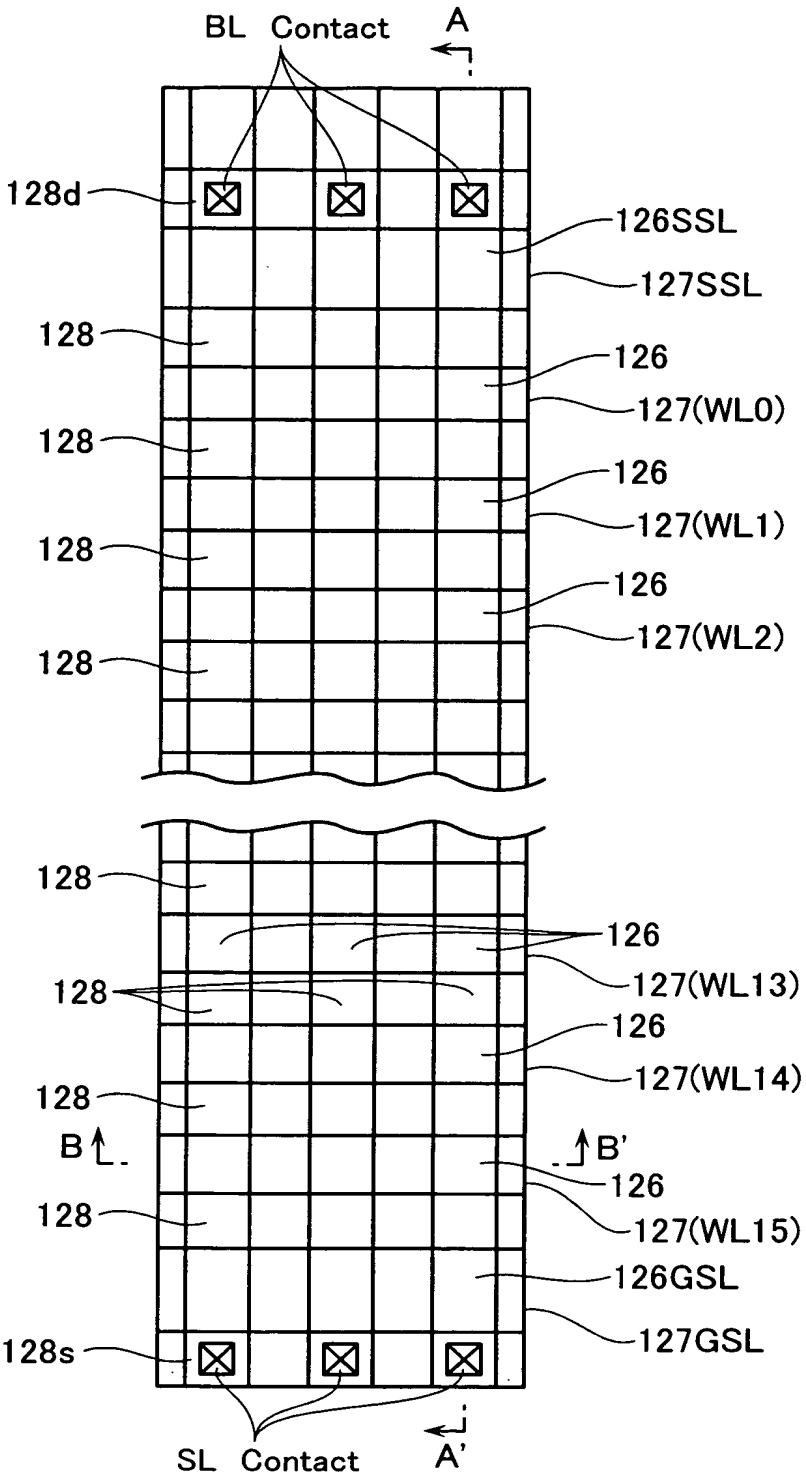

BL Contact
A
128d
126SSL
127SSL
128
126
127(WL0)
128
126
127(WL1)
128
126
127(WL2)
128
126
128
127(WL13)
126
128
127(WL14)
B
B'
126
128
127(WL15)
126GSL
128s
127GSL
SL Contact
A'

FIG. 36

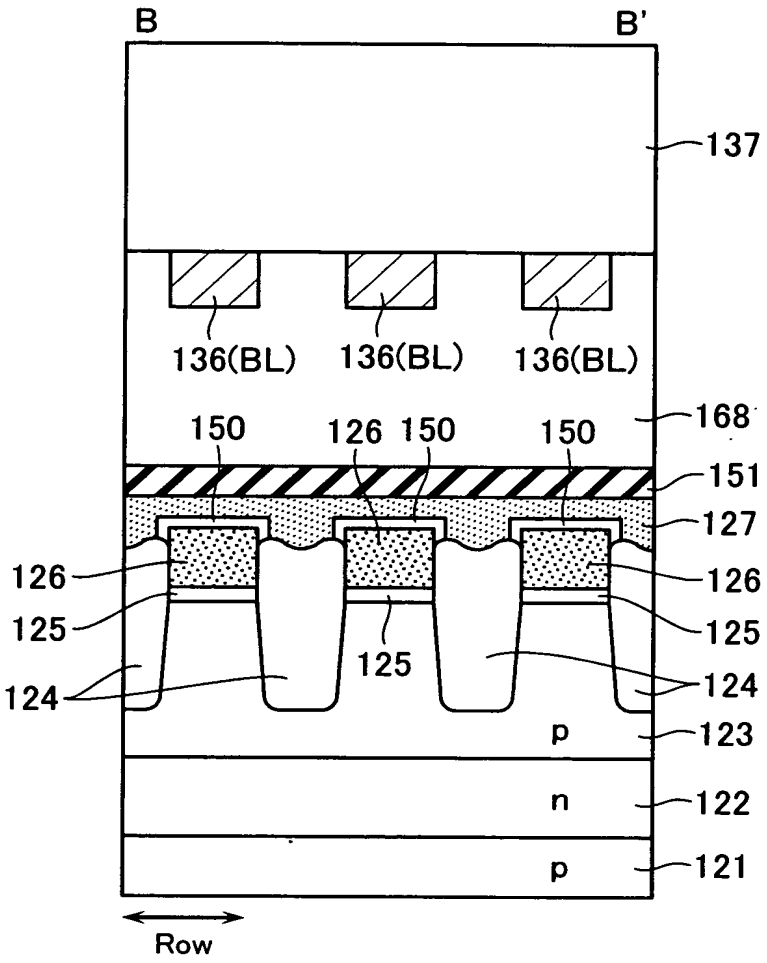

B
B'
137
136(BL)
136(BL)
136(BL)
150
126
150
150
168
151
127
126
126
125
125
125
124
124
p
123
n
122
p
121
Row

FIG. 37

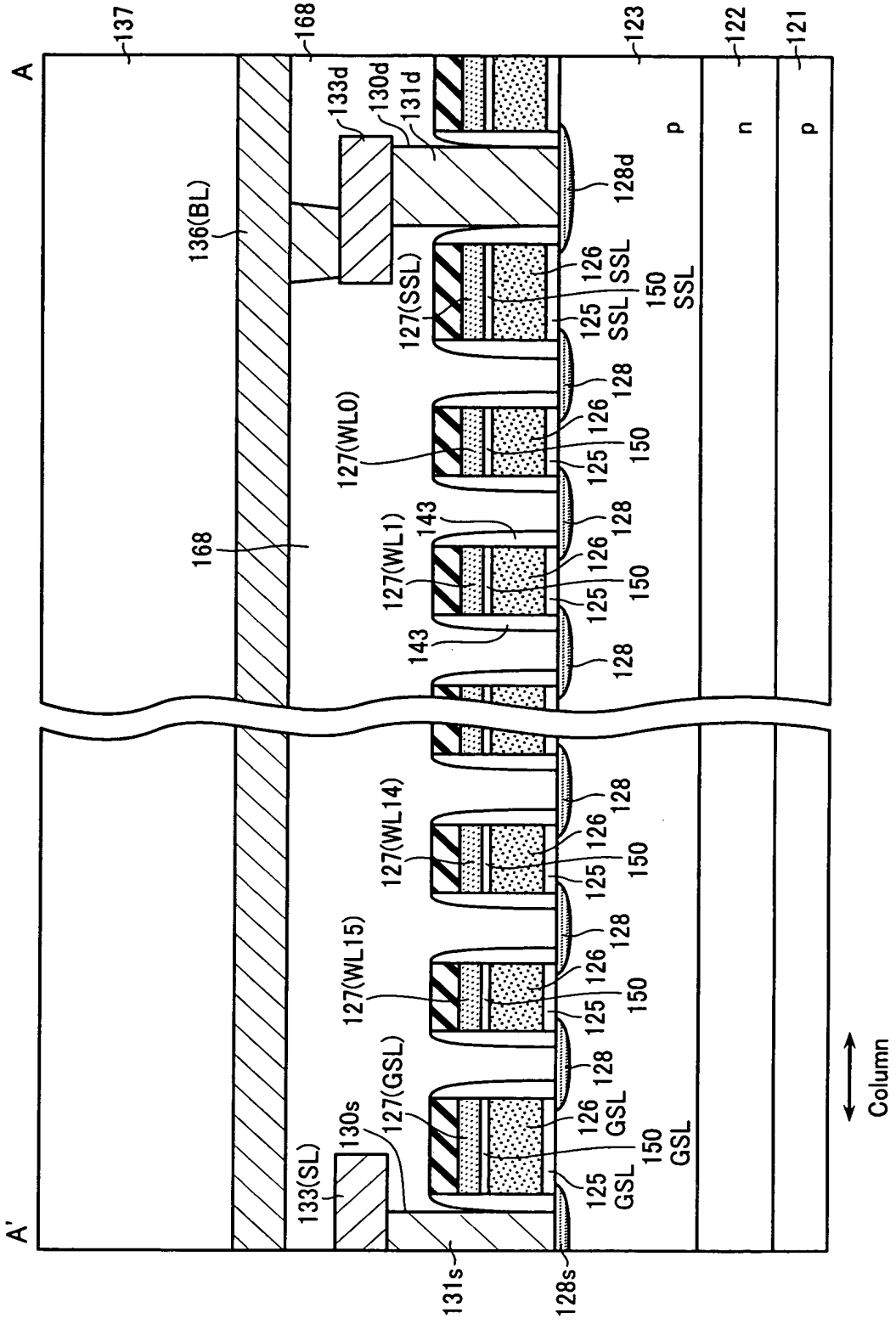

A
A'
137
168
123
122
121
p
n
p
136(BL)
168
133d
130d
131d
128d
127(SSL)
126
SSL
125
SSL
150
SSL
128
127(WL0)
126
125
150
143
127(WL1)
126
125
150
128
143
128
127(WL14)
126
125
150
128
127(WL15)
126
125
150
128
127(GSL)
126
GSL
125
GSL
150
GSL
128
130s
133(SL)
131s
128s
Column

FIG. 38

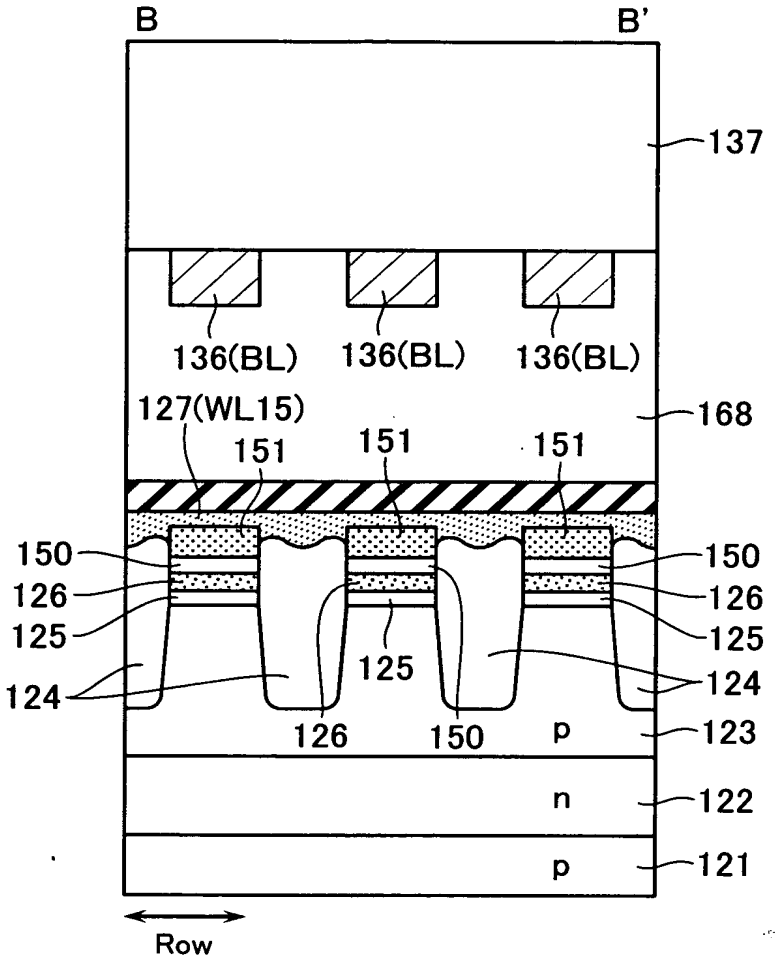

B
B'
137
136(BL)
136(BL)
136(BL)
127(WL15)
168
151
151
151
150
126
125
124
125
124
126
150
150
126
125
p
123
n
122
p
121
Row

FIG. 39

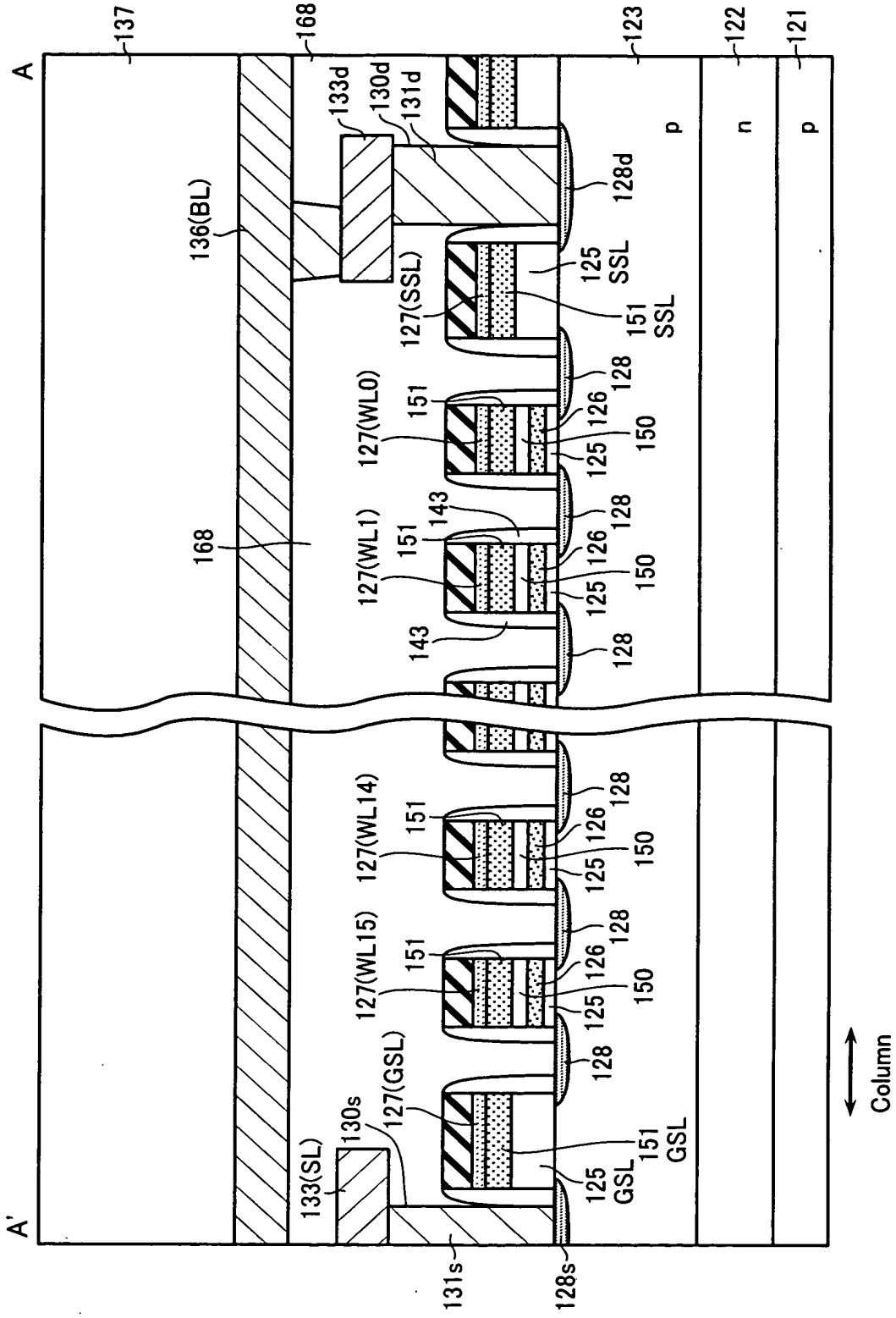

A
A'
137
168
123
122
121
p
n
p
136(BL)
168
133d
130d
131d
128d
125
SSL
151
SSL
127(SSL)
127(WL0)
151
126
128
125
150
127(WL1)
151
143
126
128
125
150
143
128
127(WL14)
151
126
128
125
150
127(WL15)
151
126
128
125
150
128
127(GSL)
130s
133(SL)
125
GSL
151
GSL
131s
128s
Column

FIG. 40

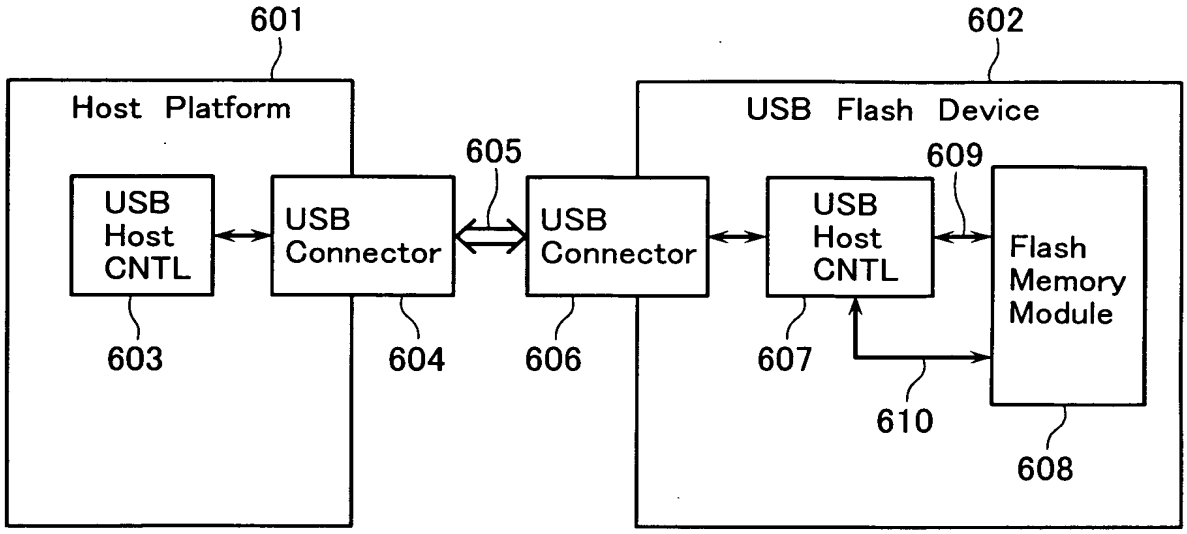

601
602
Host Platform
USB Flash Device
605
609
USB Host CNTL
USB Connector
USB Connector
USB Host CNTL
Flash Memory Module
603
604
606
607
610
608

FIG. 41

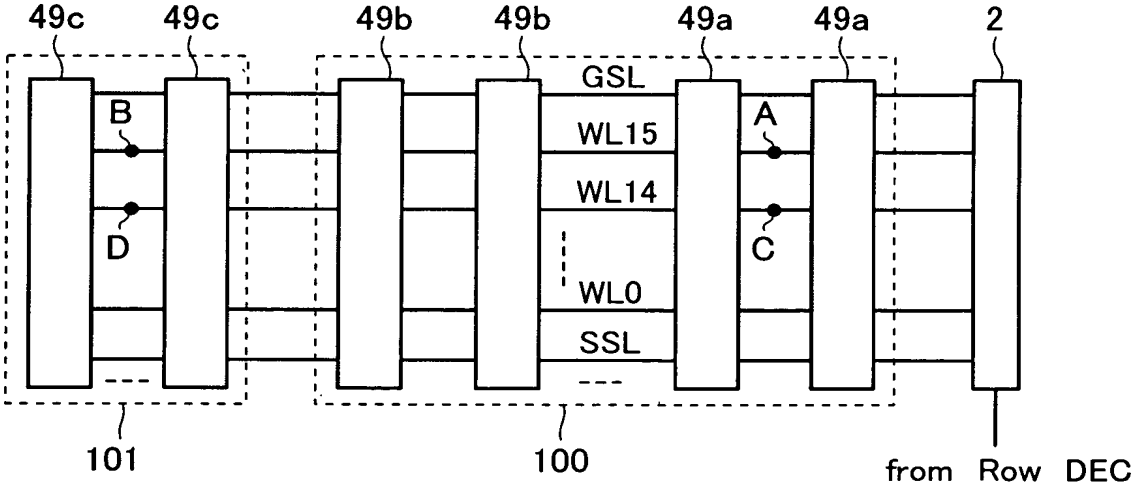
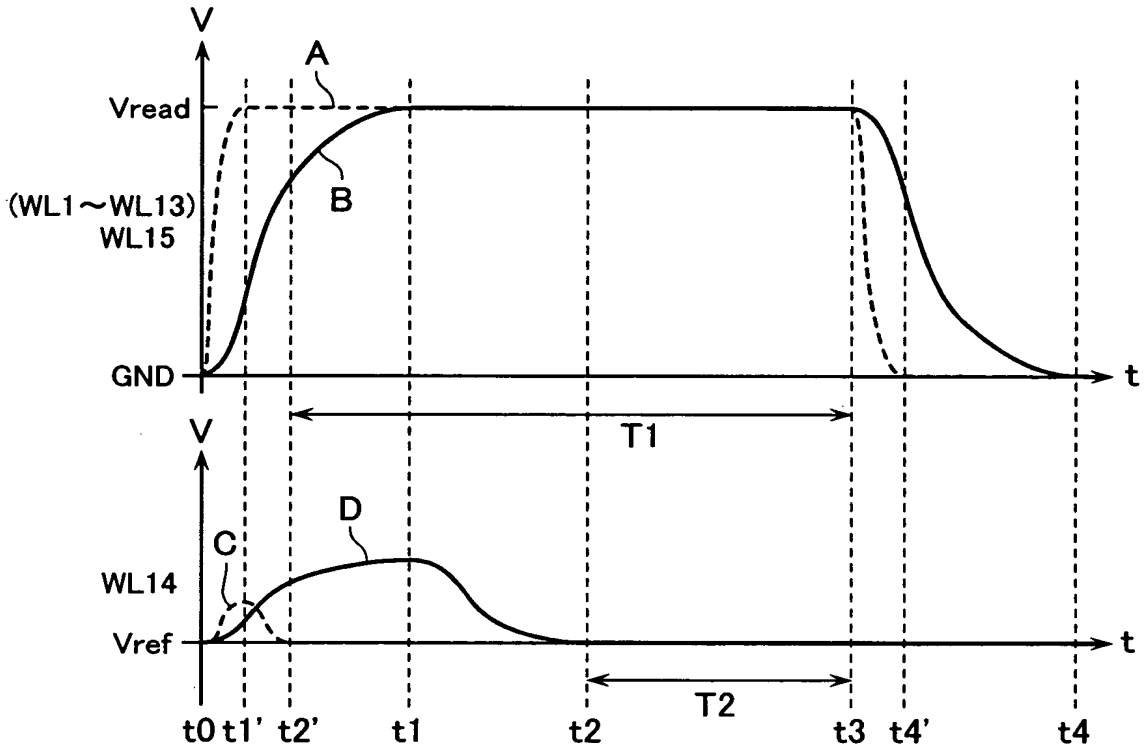

49c
49c
49b
49b
49a
49a
2
GSL
B
WL15
A
WL14
D
C
WL0
SSL
101
100
from Row DEC

FIG. 42


V
A
Vread
B
(WL1~WL13)
WL15
GND
t
T1
V
D
C
WL14
Vref
t
T2
t0 t1' t2' t1 t2 t3 t4' t4